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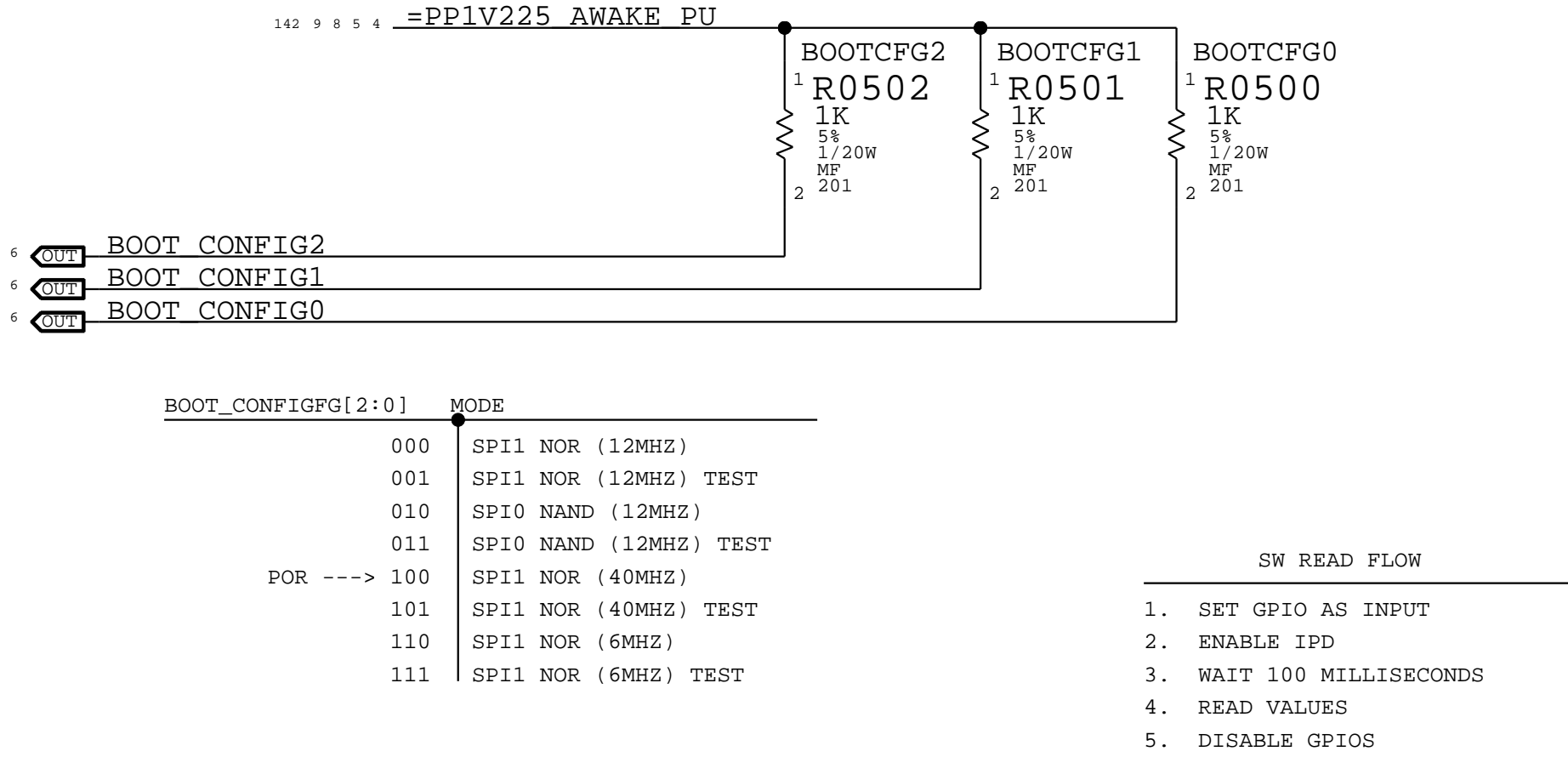
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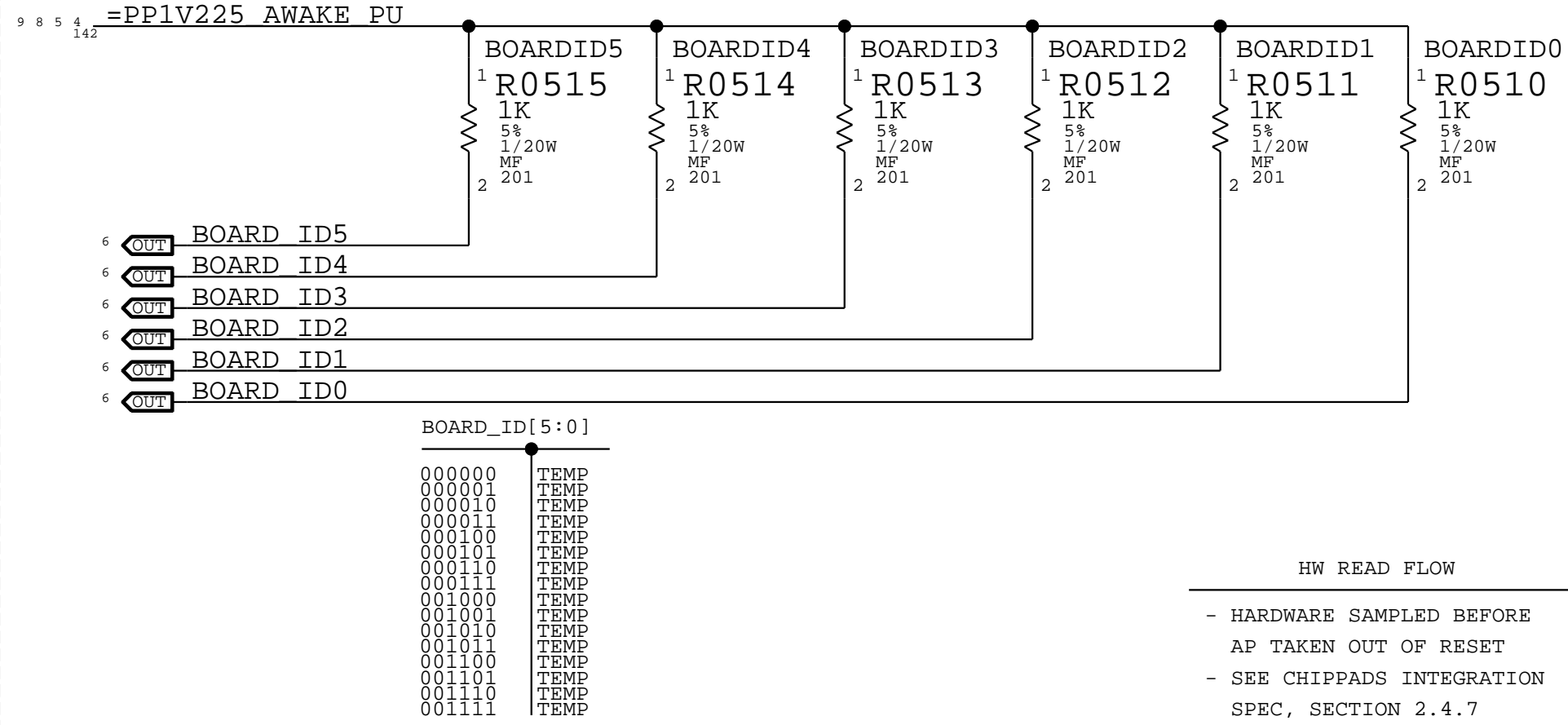
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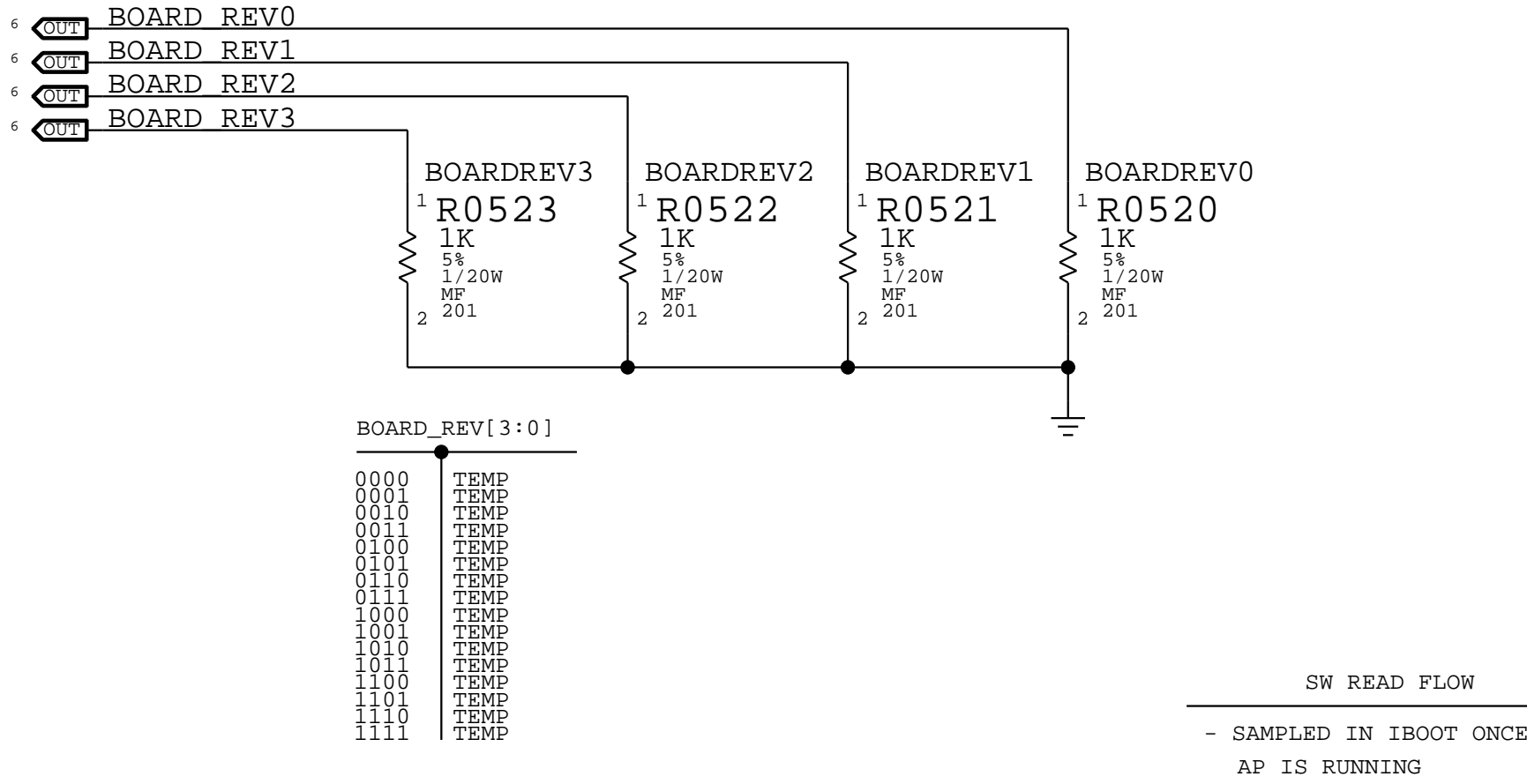
BOOT CONFIG




BOARD ID

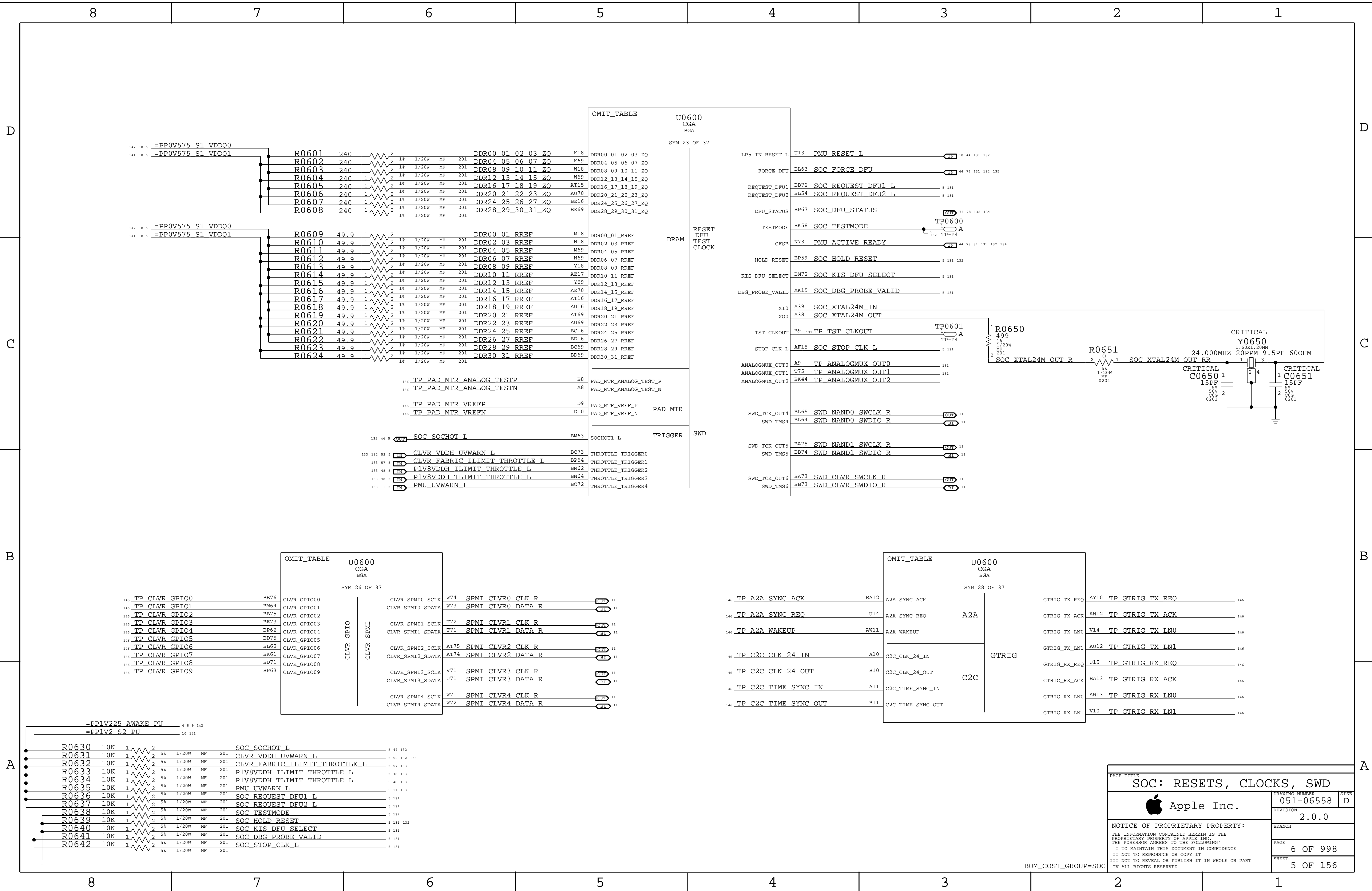


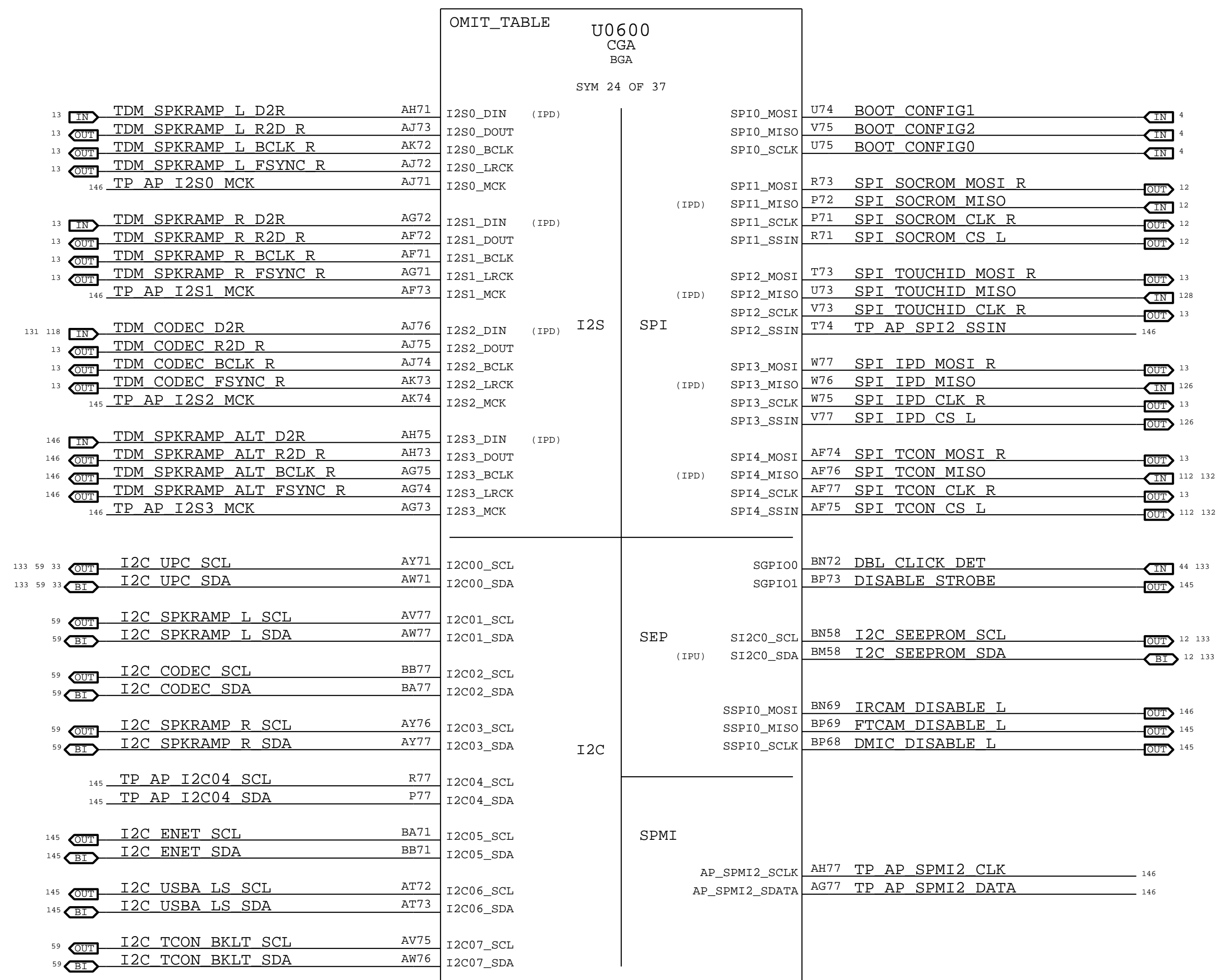
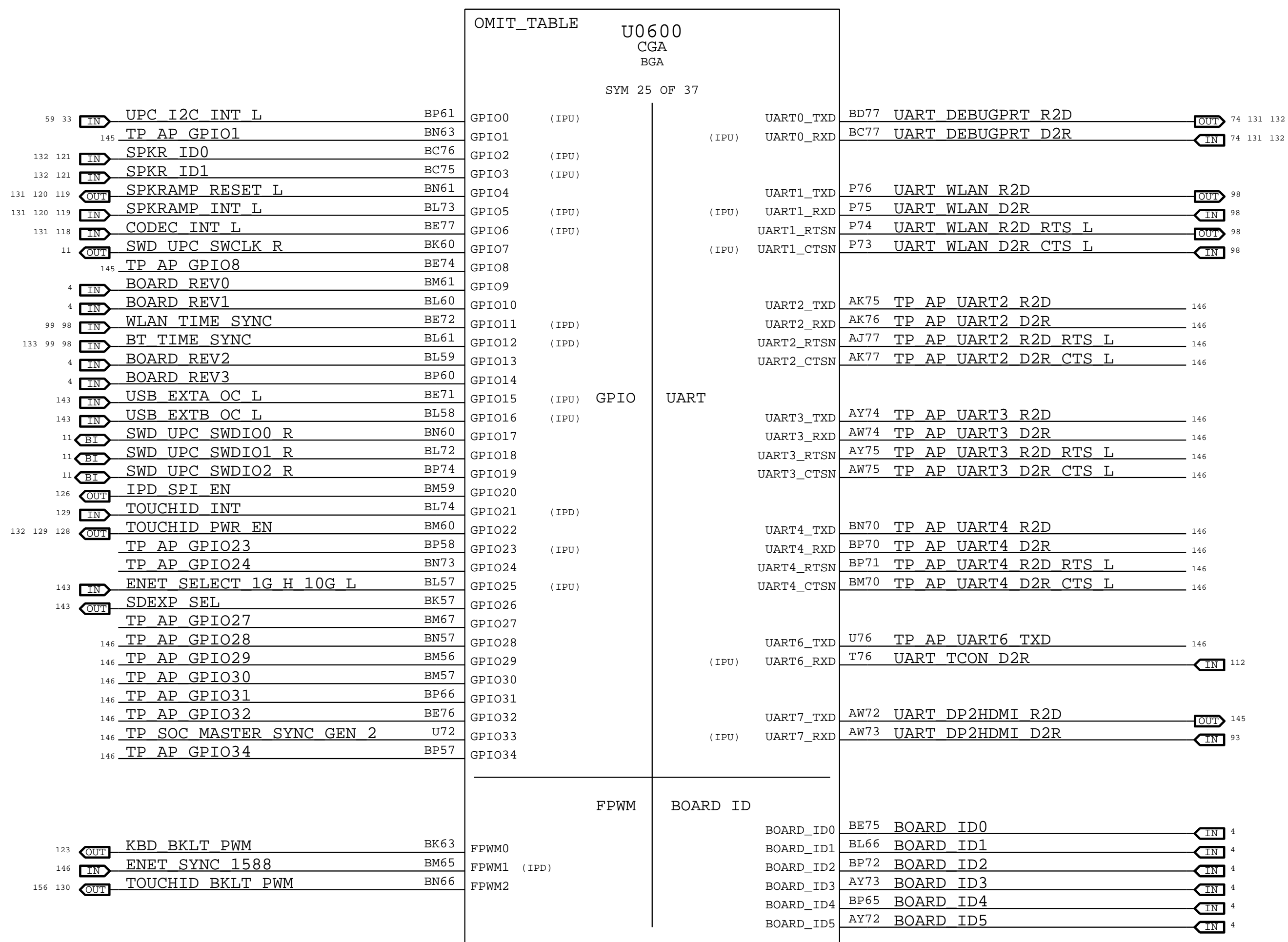
BOARD REV



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	REVISION	2.0.0
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6

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1

111

TP

LPDP FTCAM DATA P<0>

A65

LPDPRX_RX_D0_P

LPDP RX

LPDPTX0_TX0_P

B56 LPDP INT ML DATA C P<0>

143

111

TP

LPDP FTCAM DATA N<0>

B65

LPDPRX_RX_D0_N

LPDPTX0_TX0_N

A56 LPDP INT ML DATA C N<0>

143

143

TP

LPDP FTCAM DATA P<1>

A67

LPDPRX_RX_D1_P

LPDP RX

LPDPTX0_TX1_P

B57 LPDP INT ML DATA C P<1>

143

143

TP

LPDP FTCAM DATA N<1>

B67

LPDPRX_RX_D1_N

LPDPTX0_TX1_N

A57 LPDP INT ML DATA C N<1>

143

111

BT

LPDP FTCAM AUX C

D61

LPDPRX_AUX_D0_P

146

TP

LPDP FTCAM AUX

E61

LPDPRX_AUX_D1_P

LPDPTX0_TX2_P

B58 LPDP INT ML DATA C P<2>

143

LPDPTX0_TX2_N

A58 LPDP INT ML DATA C N<2>

143

LPDPTX0_TX3_P

B59 LPDP INT ML DATA C P<3>

143

LPDPTX0_TX3_N

A59 LPDP INT ML DATA C N<3>

143

LPDPTX0_AUX_P

D57 LPDP INT ML AUX C P

143

LPDPTX0_AUX_N

E57 LPDP INT ML AUX C N

143

145

TP

LPDP INT ML HPD

AU74

DISP_HP0 (IPD)

LPDP TX

LPDPTX1_TX0_P

B63 LPDP INT SL DATA C P<0>

143

143

TP

LPDP INT SL HPD

AV71

DISP_HP1 (IPD)

LPDP TX

LPDPTX1_TX0_N

A63 LPDP INT SL DATA C N<0>

143

146

TP

DISP POL

BC71

DISP_POL

LPDP TX

LPDPTX1_TX1_P

B62 LPDP INT SL DATA C P<1>

143

LPDPTX1_TX1_N

A62 LPDP INT SL DATA C N<1>

143

LPDPTX1_TX2_P

B61 LPDP INT SL DATA C P<2>

143

LPDPTX1_TX2_N

A61 LPDP INT SL DATA C N<2>

143

LPDPTX1_TX3_P

B60 LPDP INT SL DATA C P<3>

143

LPDPTX1_TX3_N

A60 LPDP INT SL DATA C N<3>

143

LPDPTX1_AUX_P

E60 LPDP INT SL AUX C P

143

LPDPTX1_AUX_N

F60 LPDP INT SL AUX C N

143

146

TP

DISP TOUCH BSYNC0

BD73

DISP_TOUCH_BSYNC0

146

TP

DISP TOUCH BSYNC1

BM73

DISP_TOUCH_BSYNC1

146

TP

DISP TOUCH EB

BC74

DISP_TOUCH_EB

14

BT

BKLT BOOST THROTTLE L

AV73

DFR_BSYNC

146

TP

DFR DISP TE

BM74

DFR_DISP_TE

LPDPTX0_RCAL_P

E58 SOC LPDPTX0 RCAL P

7

LPDPTX0_RCAL_N

F58 SOC LPDPTX0 RCAL N

7

LPDPTX1_RCAL_P

E59 SOC LPDPTX1 RCAL P

7

LPDPTX1_RCAL_N

D59 SOC LPDPTX1 RCAL N

7

LPDPRX_RCAL_P

A66 SOC LPDPRX RCAL P

7

LPDPRX_RCAL_N

B66 SOC LPDPRX RCAL N

7

146

TP

ISP I2C0_SCL

BK55

ISP_I2C0_SCL

ISP_GPIO_0

BL56 FTCAM RESET L

117

146

TP

ISP I2C0_SDA

BK54

ISP_I2C0_SDA

ISP_GPIO_1

BL55 IRCAM RESET L

146

146

TP

ISP I2C1_SCL

BM68

ISP_I2C1_SCL

ISP_GPIO_2

BN67 CAM PMU RESET L

146

146

TP

ISP I2C1_SDA

BM69

ISP_I2C1_SDA

ISP_GPIO_3

BP55 TP ISP GPIO3

146

61

BT

I2C CAM_SCL

BL67

ISP_I2C2_SCL

ISP_SPMI0_SCLCK

BN55 SPMI ISP CAM CLK R

146

61

BT

I2C CAM_SDA

BL69

ISP_I2C2_SDA

ISP_SPMI0_SDATA

BM55 SPMI ISP CAM DATA R

146

146

TP

ISP I2C3_SCL

BN54

ISP_I2C3_SCL

ISP_SPMI1_SCLCK

BM53 TP SPMI1 ISP CLK

146

146

TP

ISP I2C3_SDA

BP54

ISP_I2C3_SDA

ISP_SPMI1_SDATA

BM54 TP SPMI1 ISP DATA

146

SENSOR0_CLK

BL70 CAM PMU CLK24M_R

146

SENSOR1_CLK

BM71 TP SENSOR1_CLK

146

SENSOR2_CLK

BP56 TP SENSOR2_CLK

146

SENSOR3_CLK

BM66 TP SENSOR3_CLK

146

ISP

143

BT

MIPI IRCAM_CLK_P

A74

MIPI0C_DPCLK

MIPI

D66 TP MIPID_CLKP

143

143

BT

MIPI IRCAM_CLK_N

B74

MIPI0C_DNCLK

MIPI

E66 TP MIPID_CLKN

143

143

BT

MIPI IRCAM_DATA_P<0>

A75

MIPI0C_DPDATA0

MIPI

D65 TP MIPID_DATAP

143

143

BT

MIPI IRCAM_DATA_N<0>

B75

MIPI0C_DNDATA0

MIPI

E65 TP MIPID_DATAN

143

143

BT

MIPI IRCAM_DATA_P<1>

A73

MIPI0C_DPDATA1

MIPI

143

BT

MIPI IRCAM_DATA_N<1>

B73

MIPI0C_DNDATA1

MIPI

143

BT

MIPI FTCAM_CLK_P

A70

MIPI1C_DPCLK

MIPI

143

BT

MIPI FTCAM_CLK_N

B70

MIPI1C_DNCLK

MIPI

143

BT

MIPI FTCAM_DATA_P<0>

A69

MIPI1C_DPDATA0

MIPI

143

BT

MIPI FTCAM_DATA_N<0>

B69

MIPI1C_DNDATA0

MIPI

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A71

MIPI1C_DPDATA1

MIPI

143

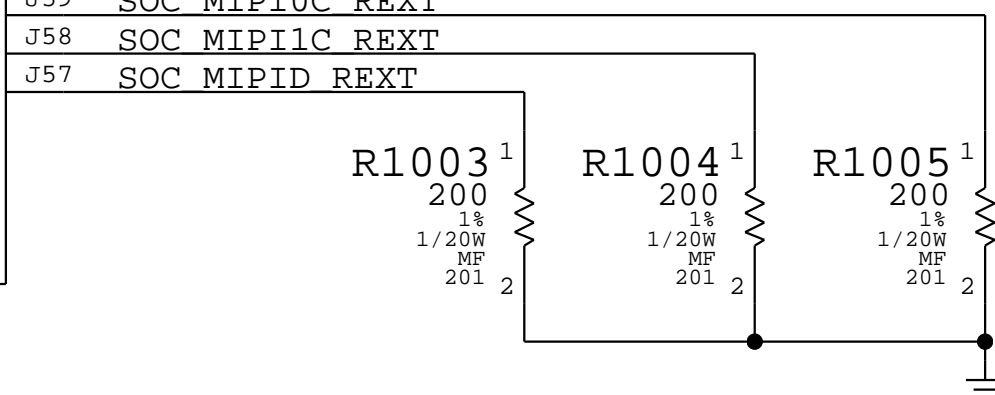
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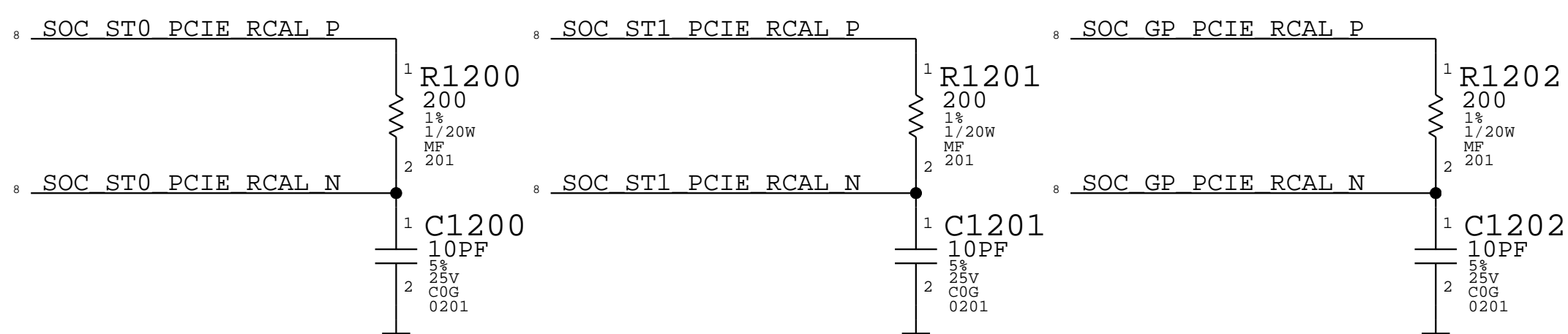
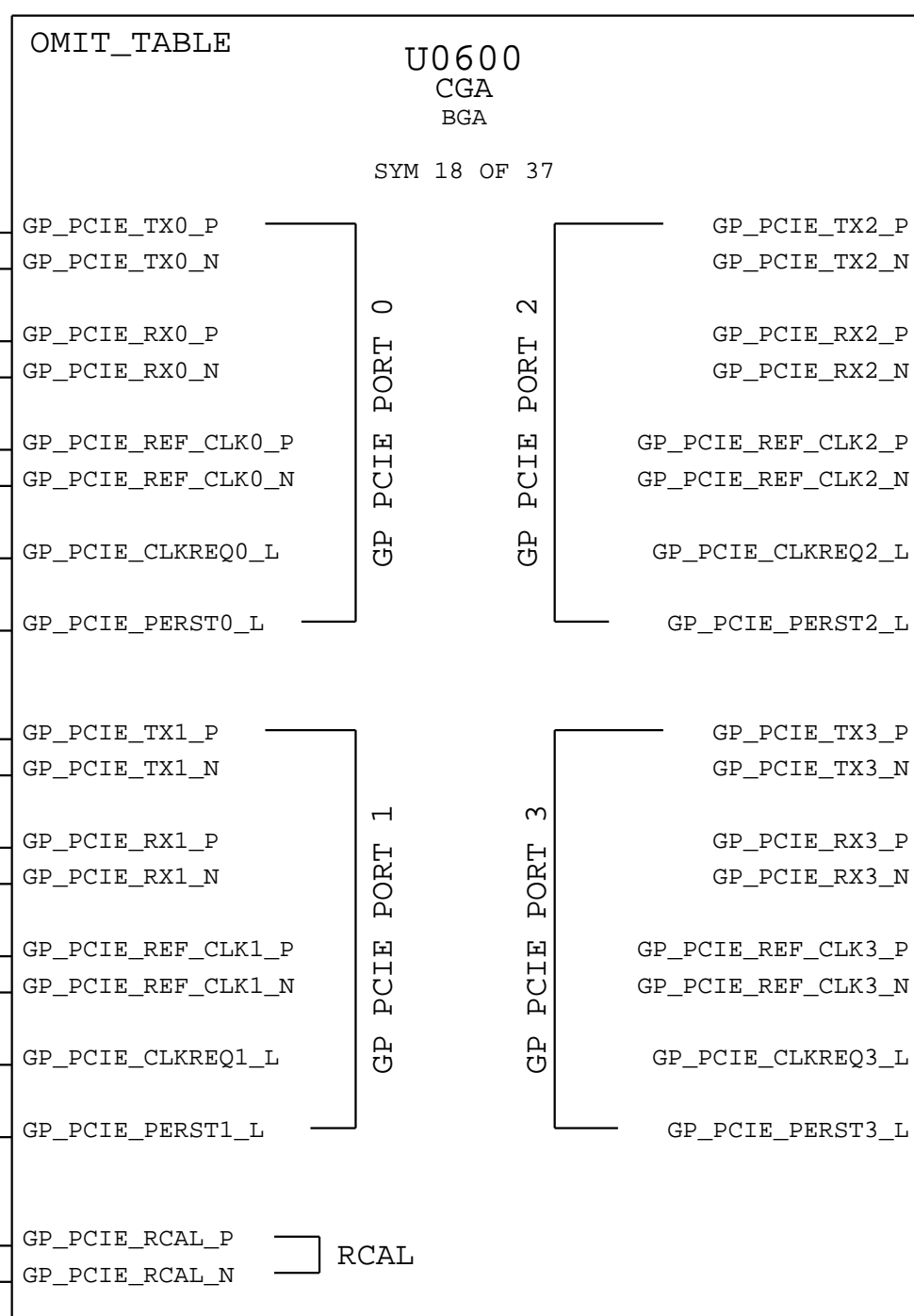
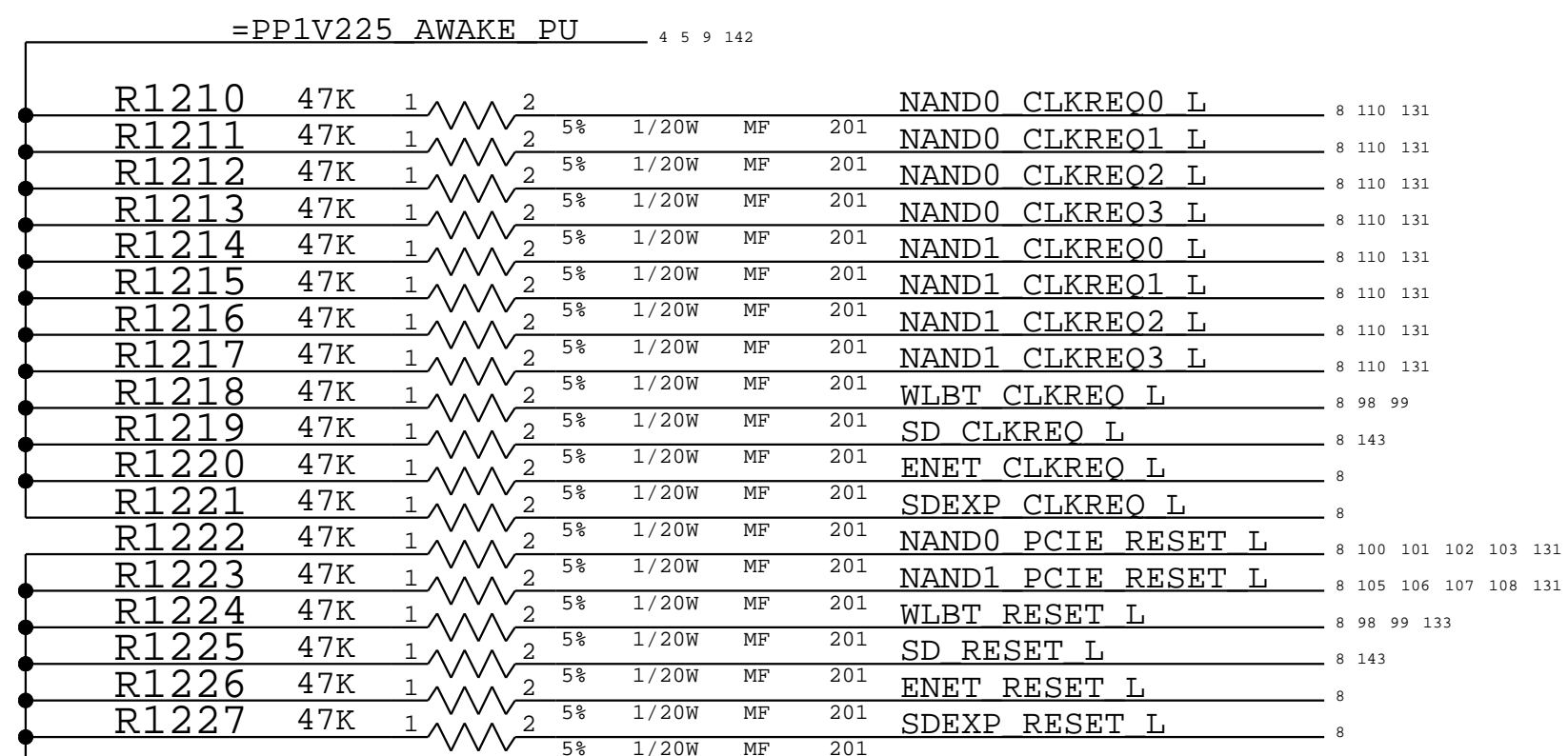
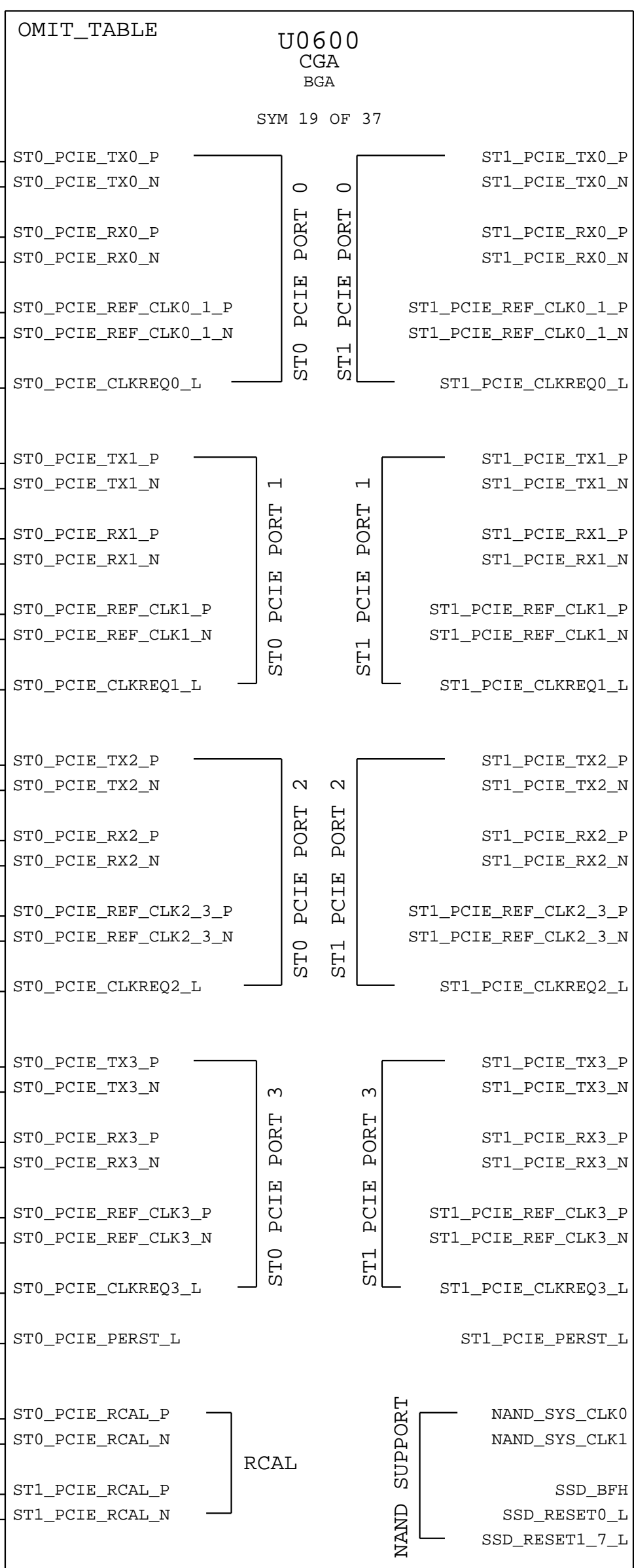
MIPI FTCAM_DATA_N<1>


B71

MIPI1C_DNDATA1

MIPI





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	051-06558		D
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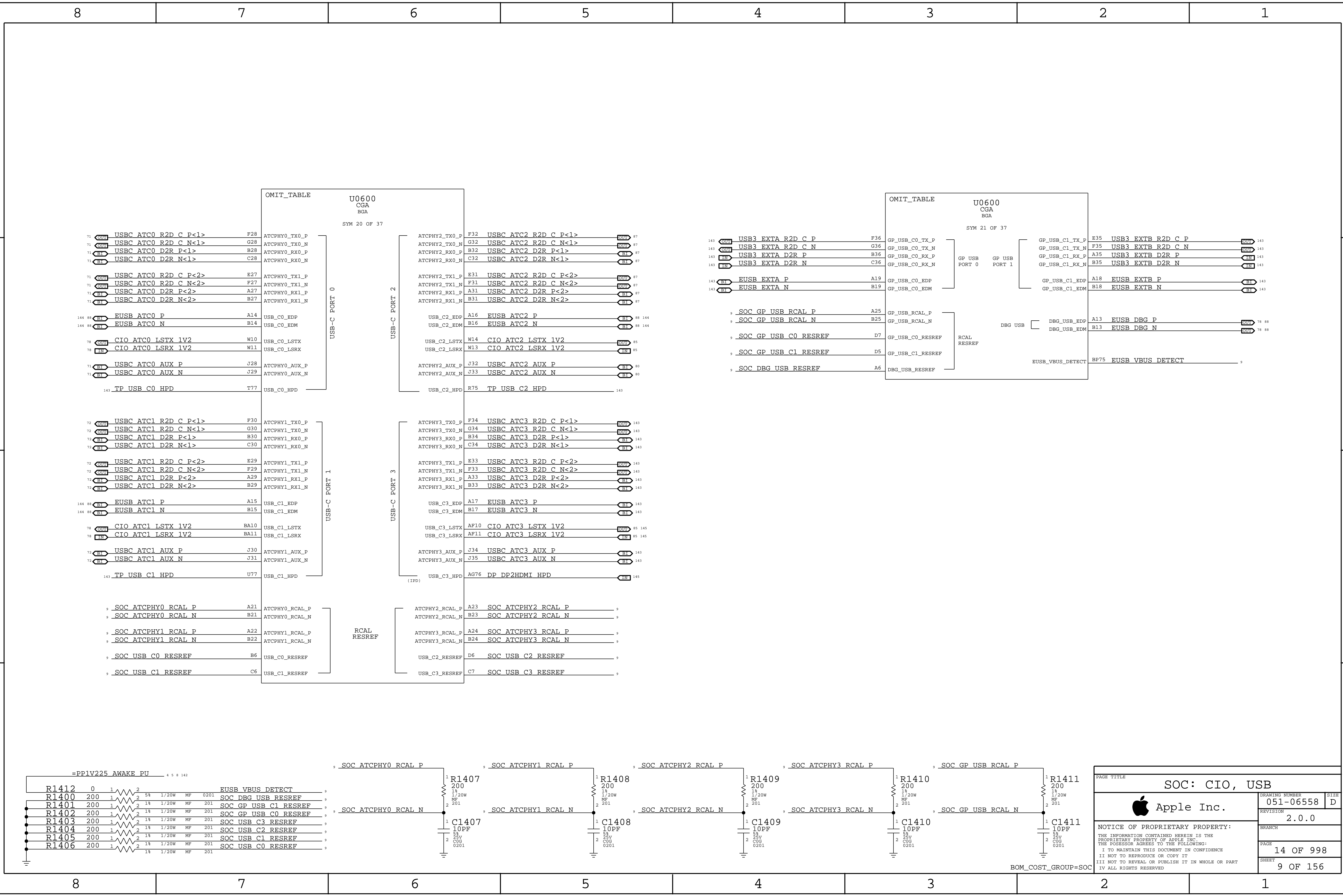
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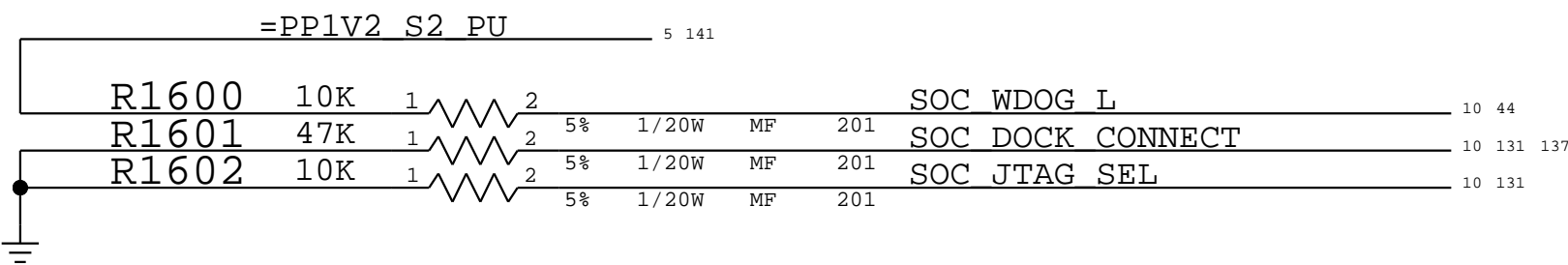
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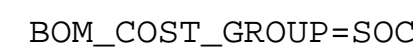
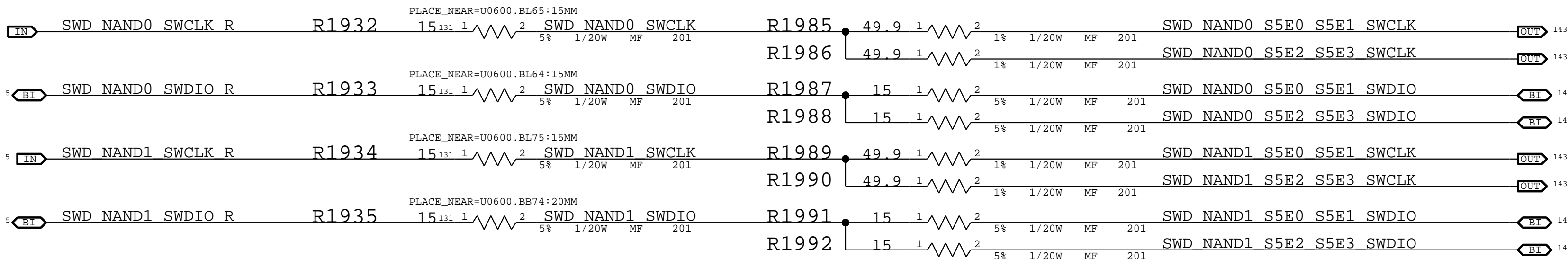
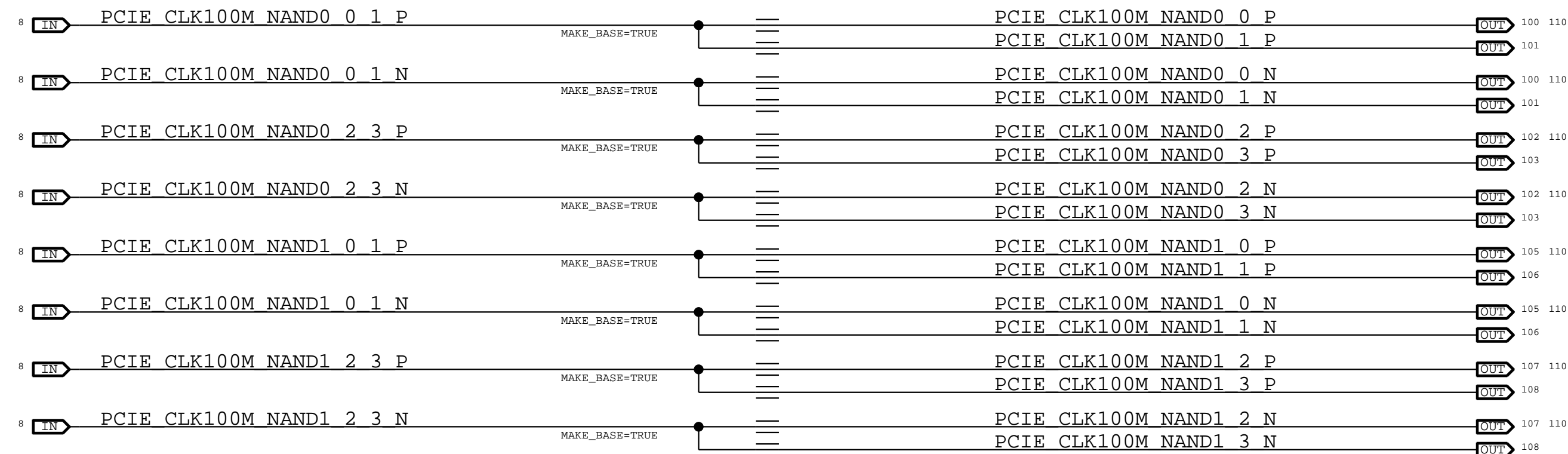
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SOC: AOP, SMC, NUB			
 Apple Inc.	DRAWING NUMBER		SIZE
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REVISION		2.0.0	
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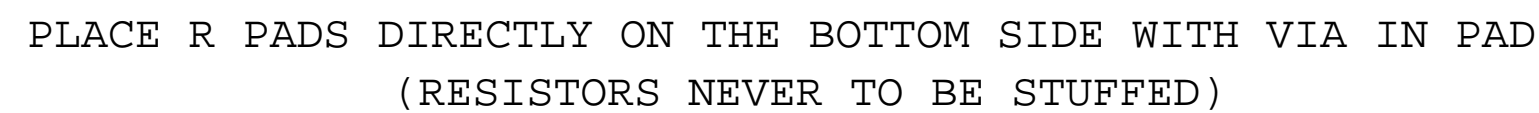
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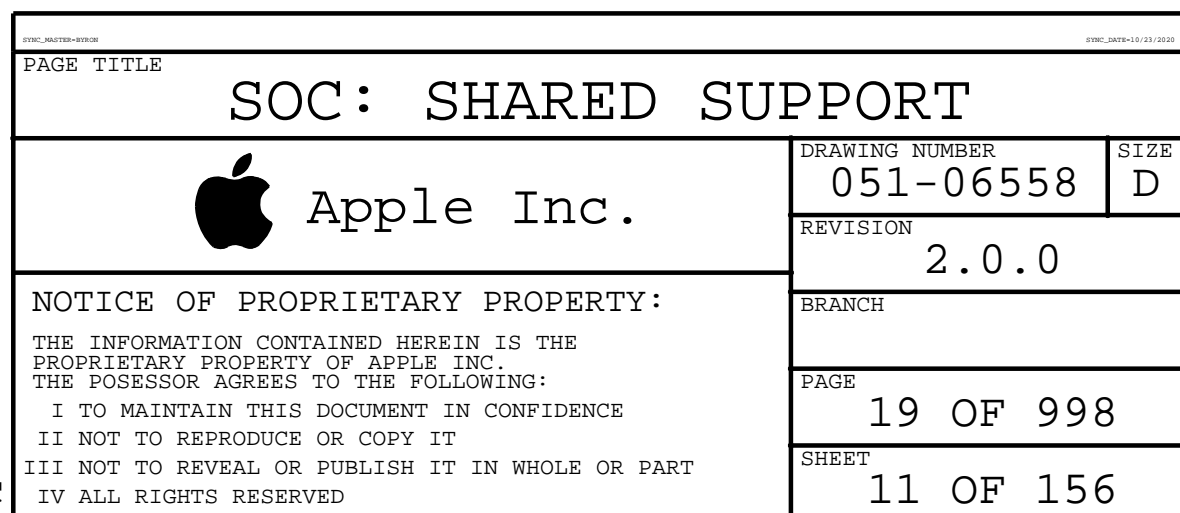
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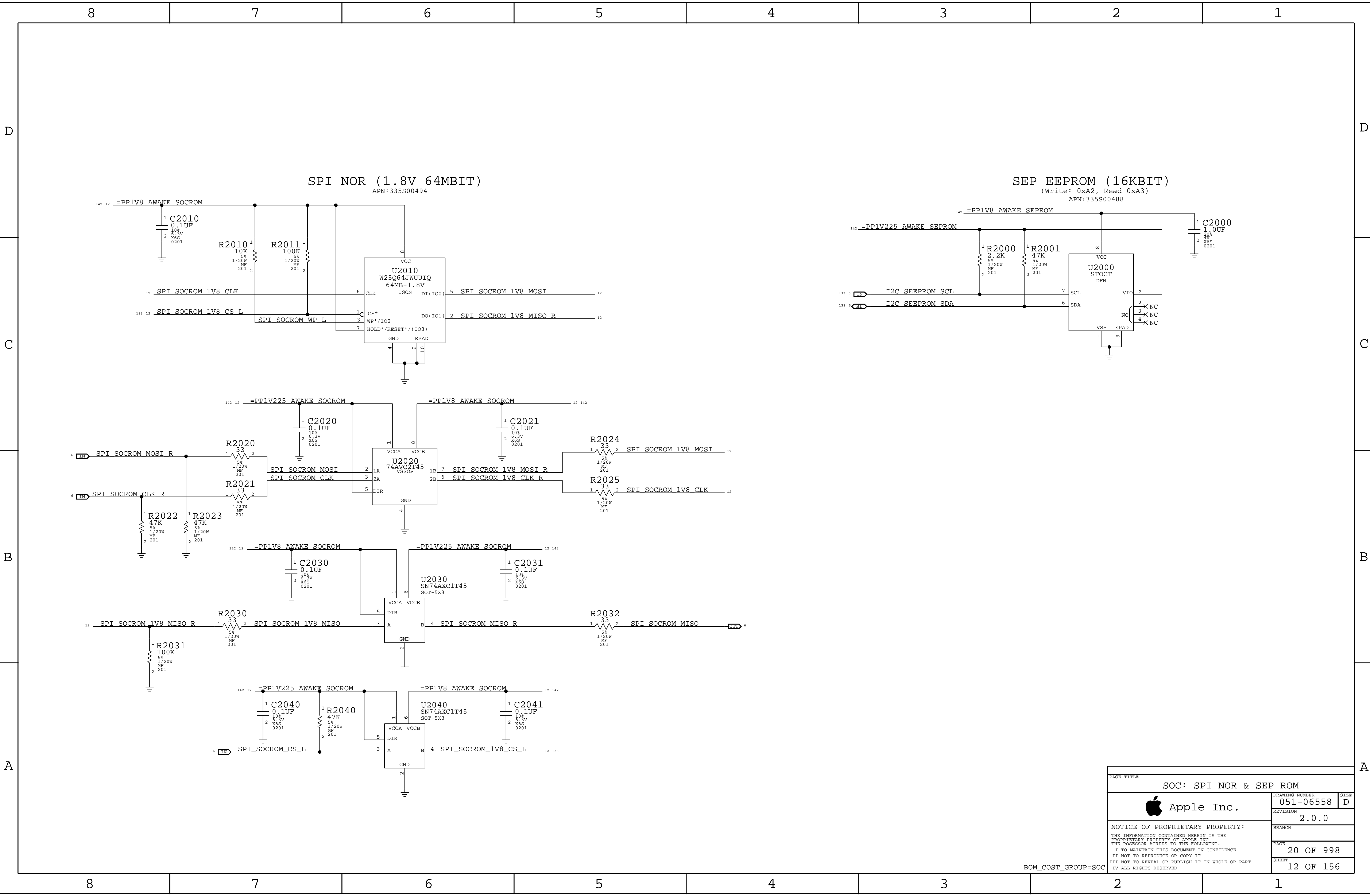



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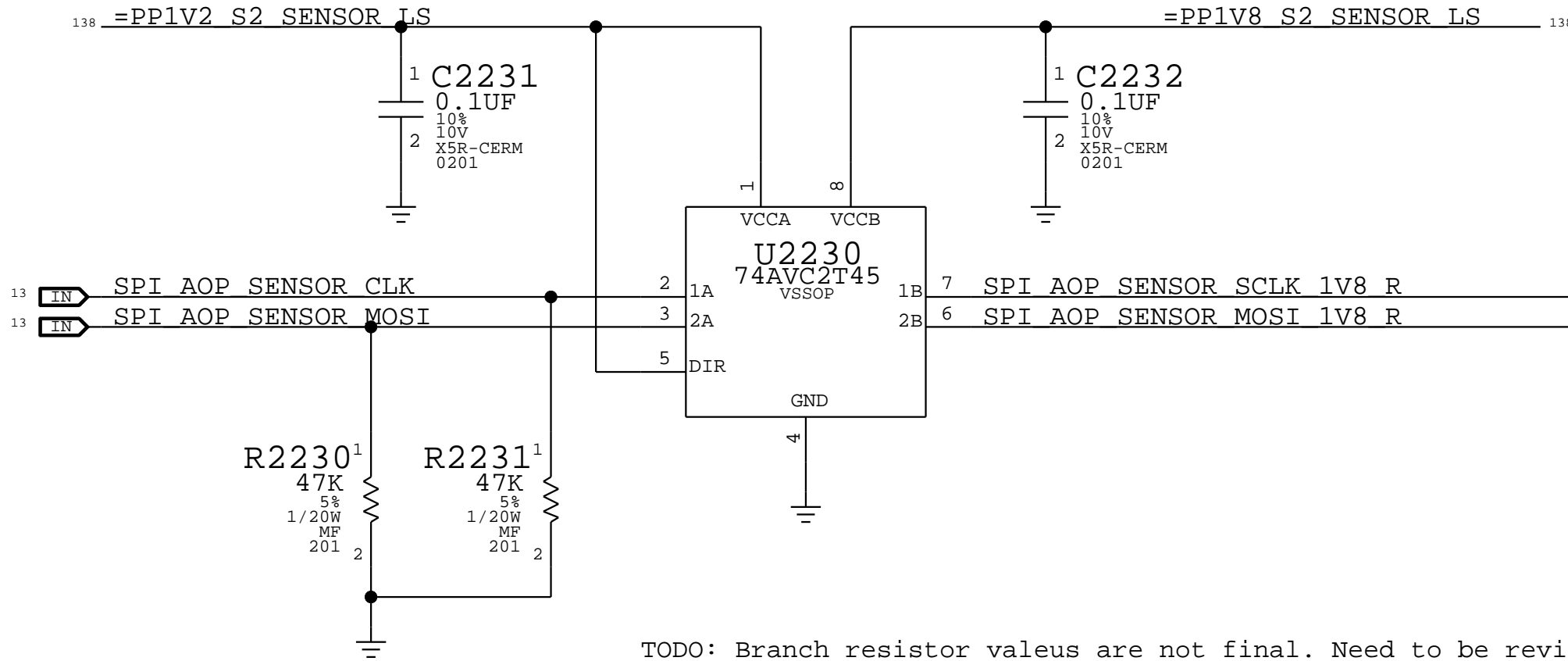
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SOC: SPI NOR & SEP ROM		
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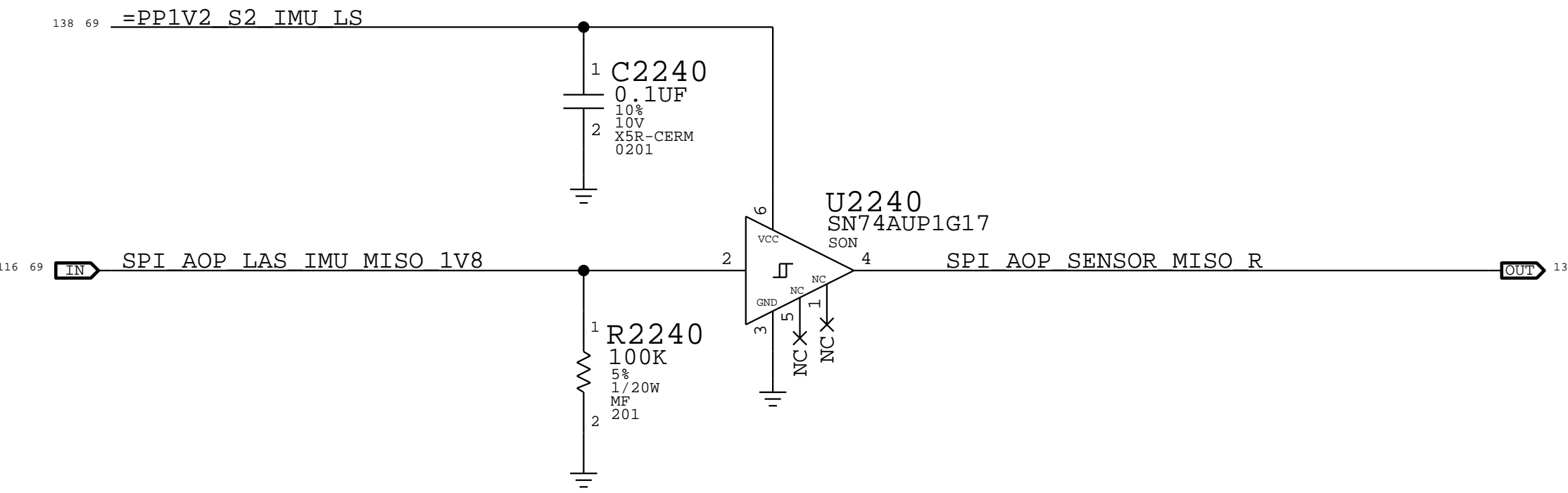
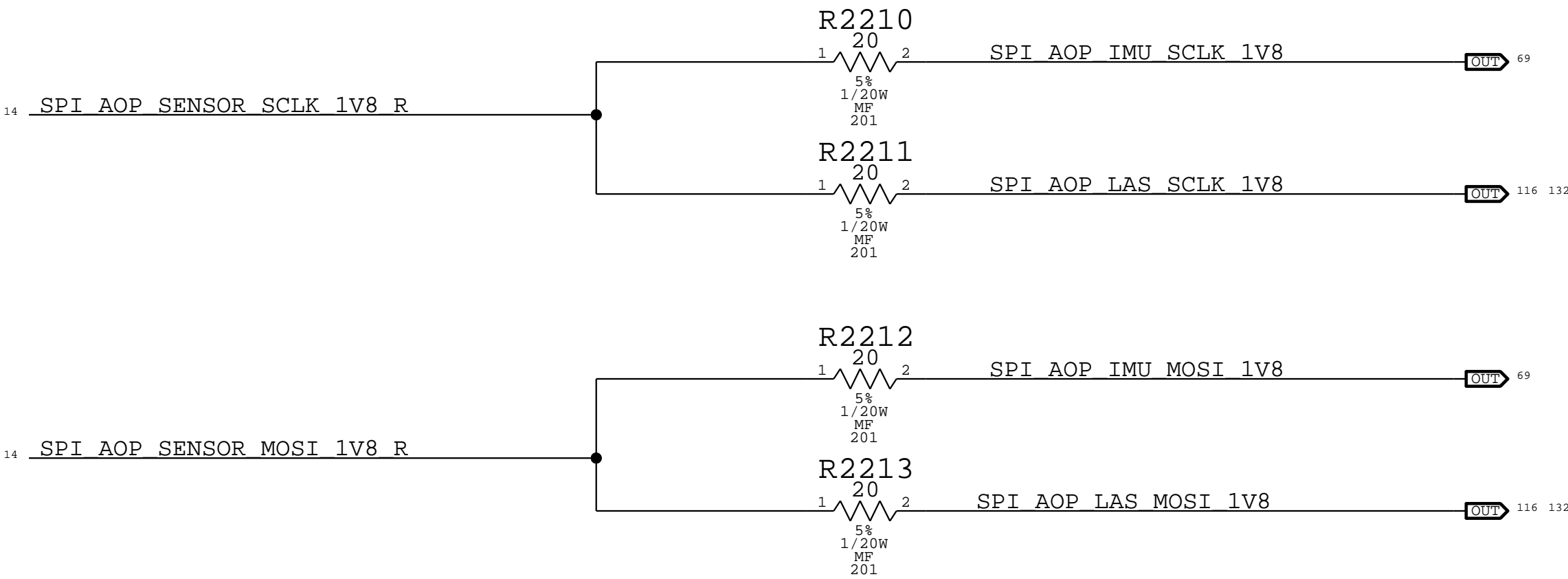
SPI AOP Sensor LS and Branch Resistors

DISPLAY BACKLIGHT

TODO: Reference designators need to be updated once layout has imported latest netlist

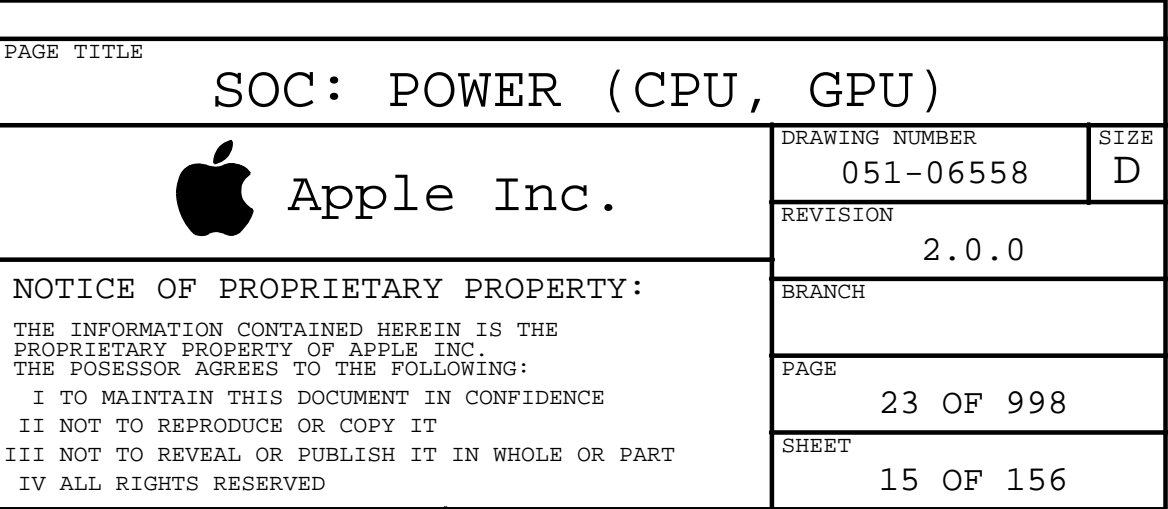


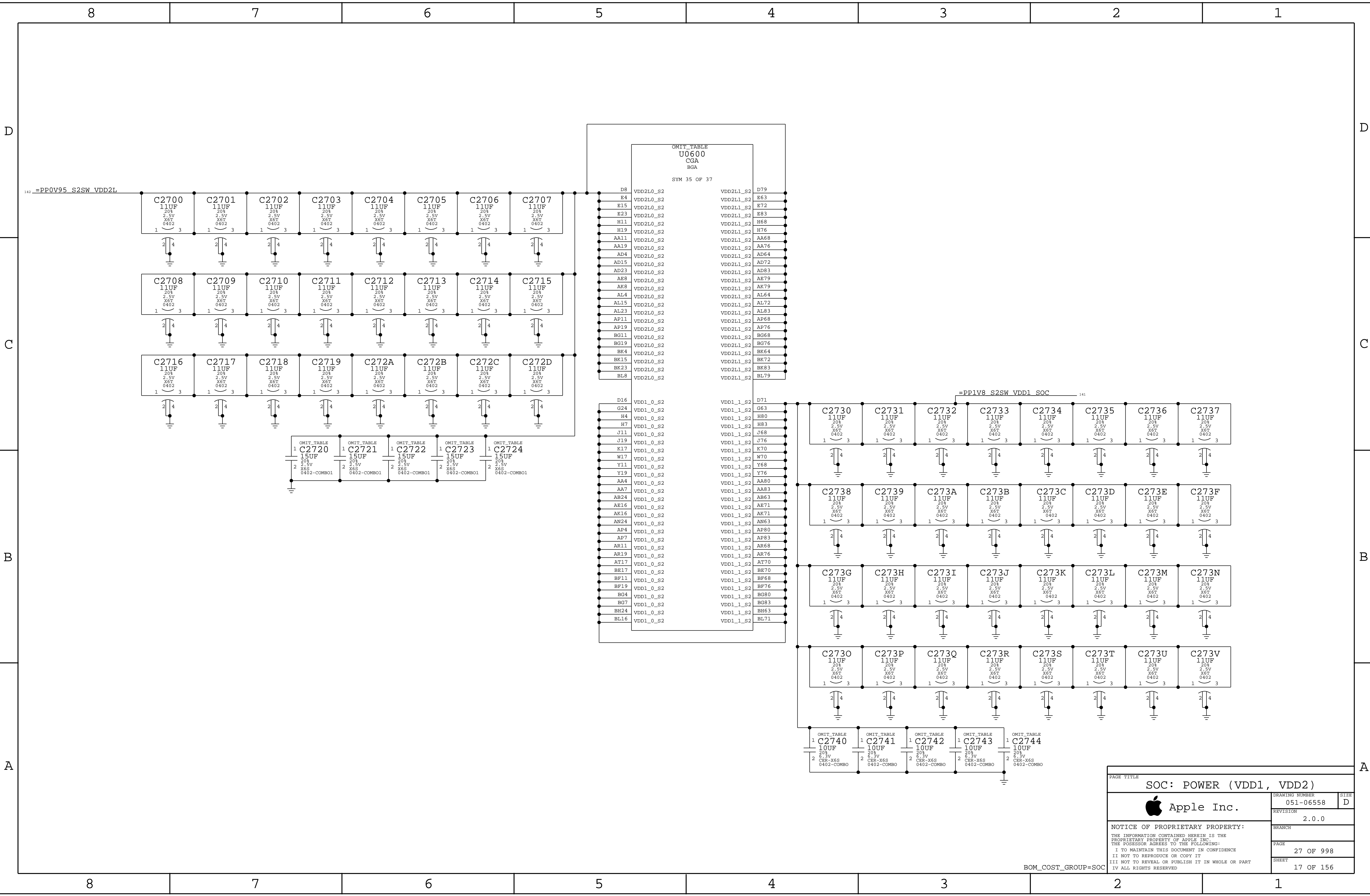
TODO: Branch resistor valeus are not final. Need to be reviewed by SI once routed




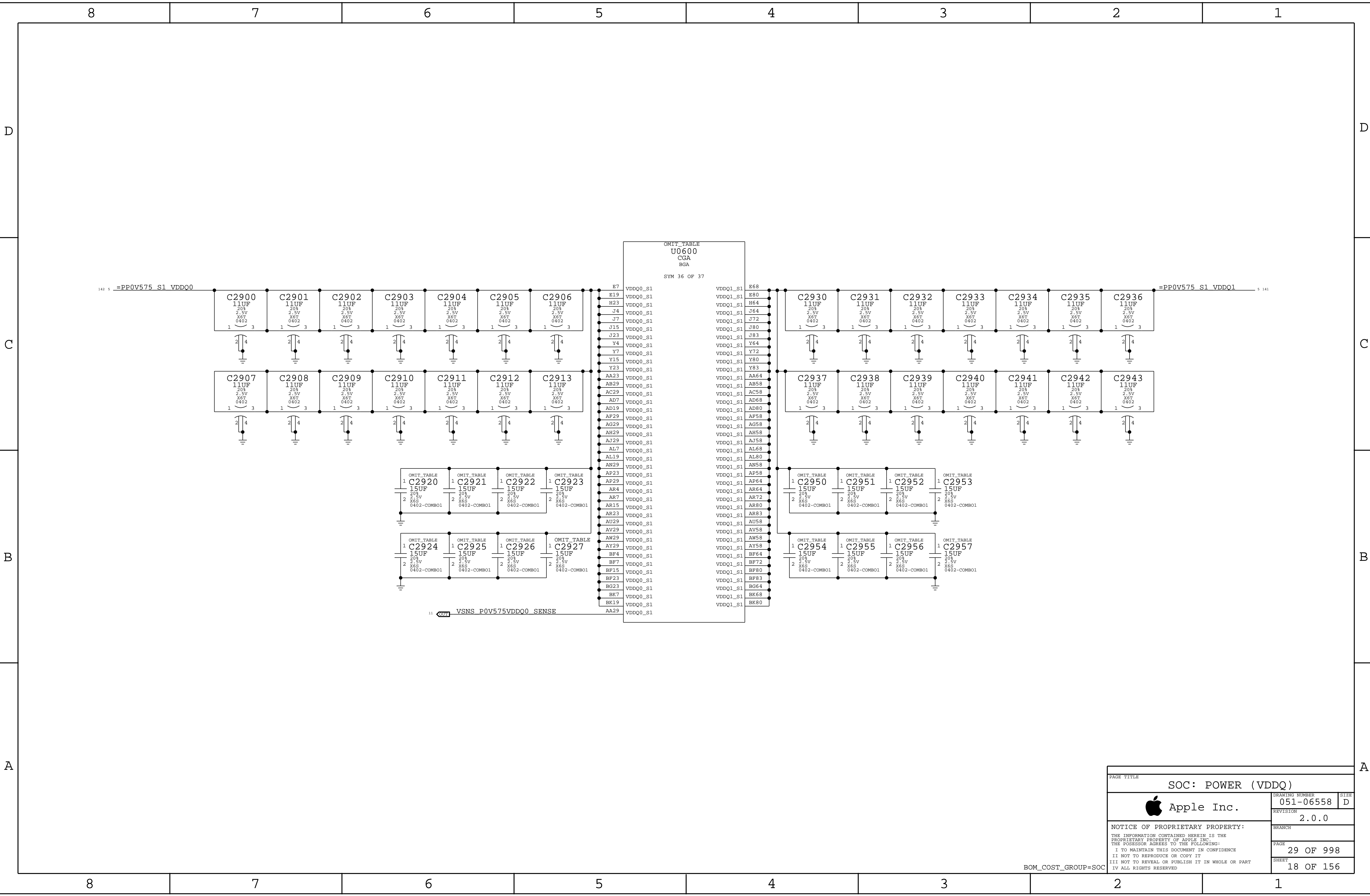
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PROJECT SUPPORT (2/2)		
Apple Inc.	DRAWING NUMBER	051-06558
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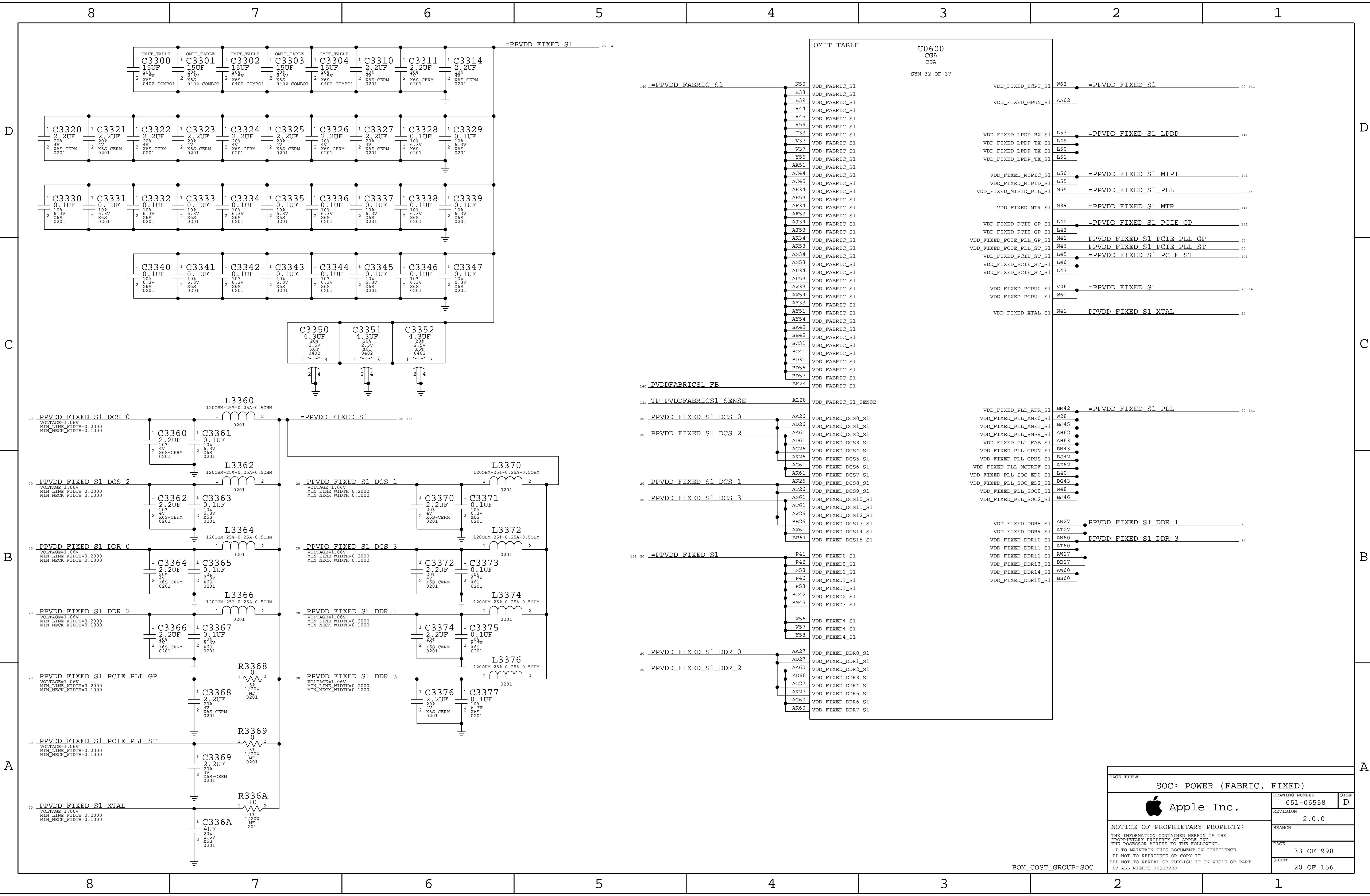


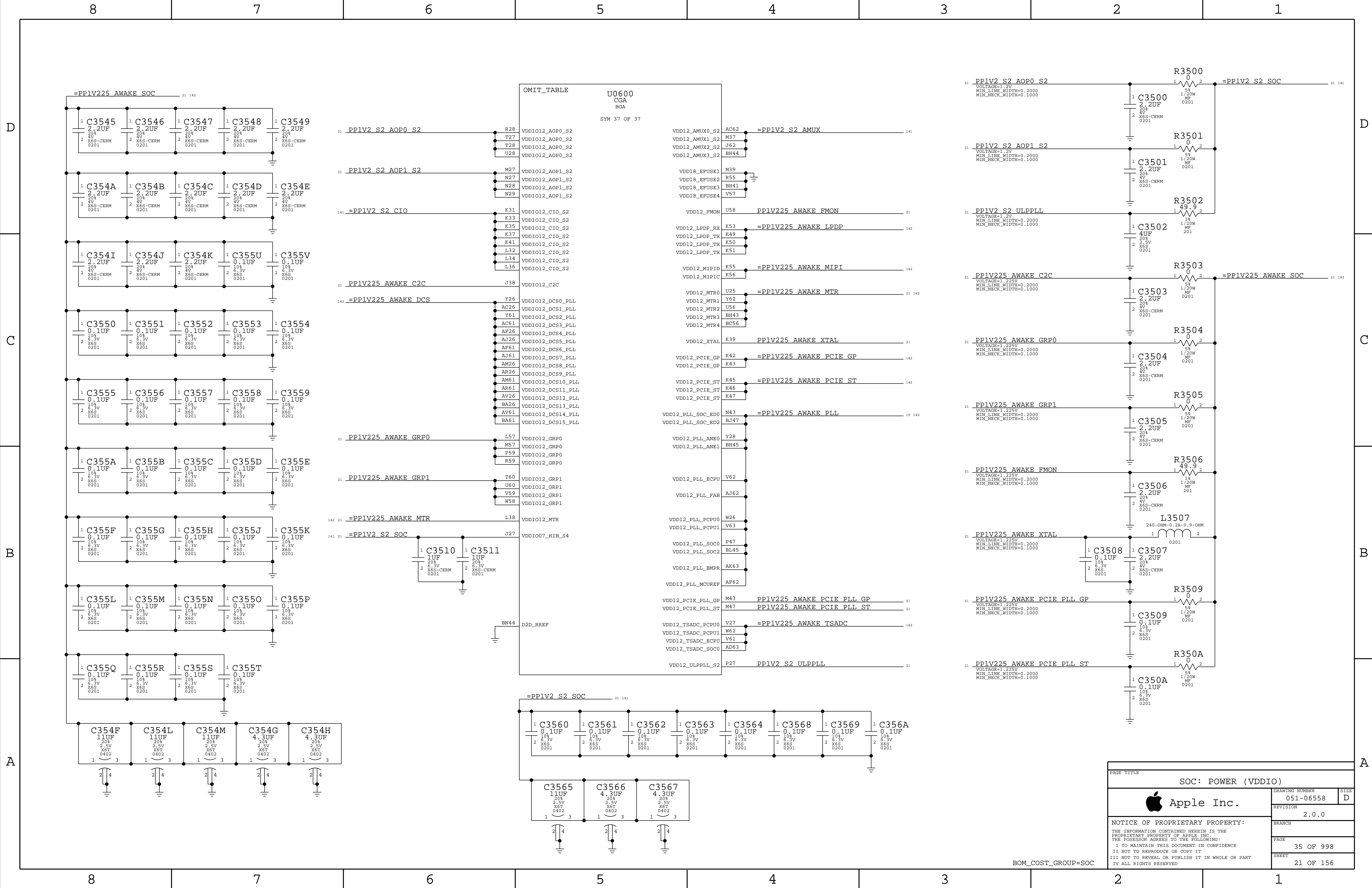
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SOC: POWER (VDD1, VDD2)		
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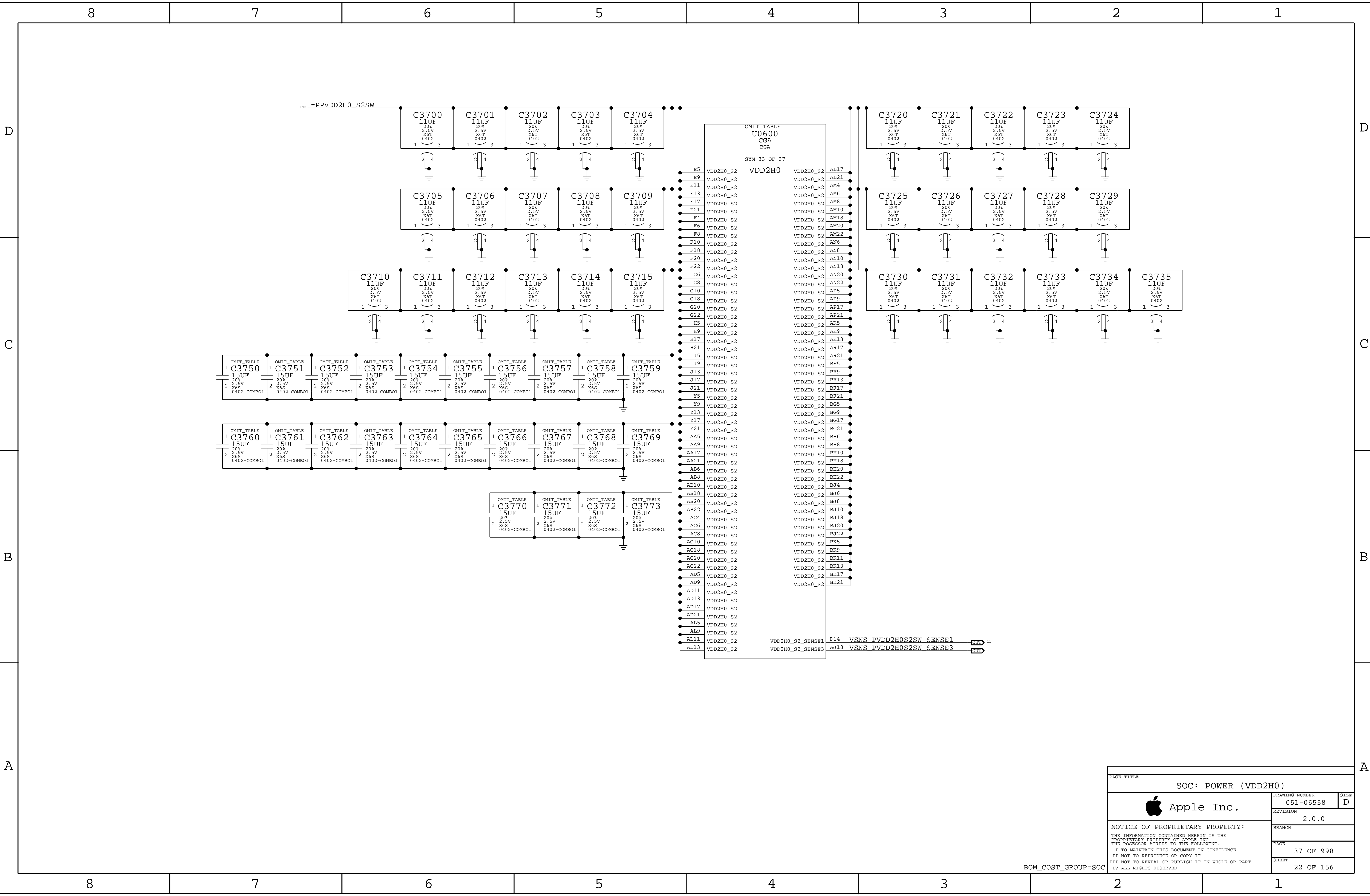


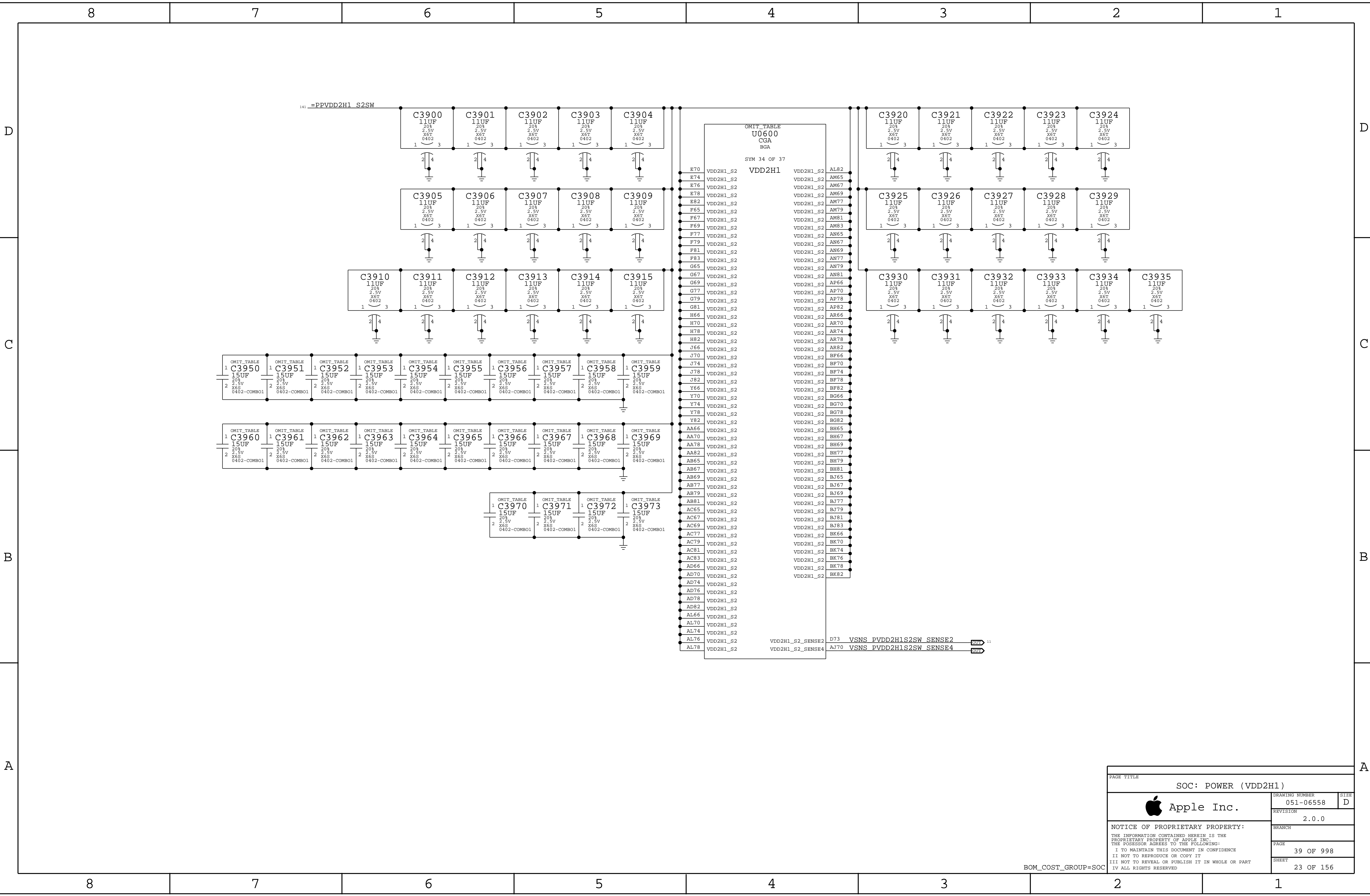
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BOM_COST_GROUP=SOC



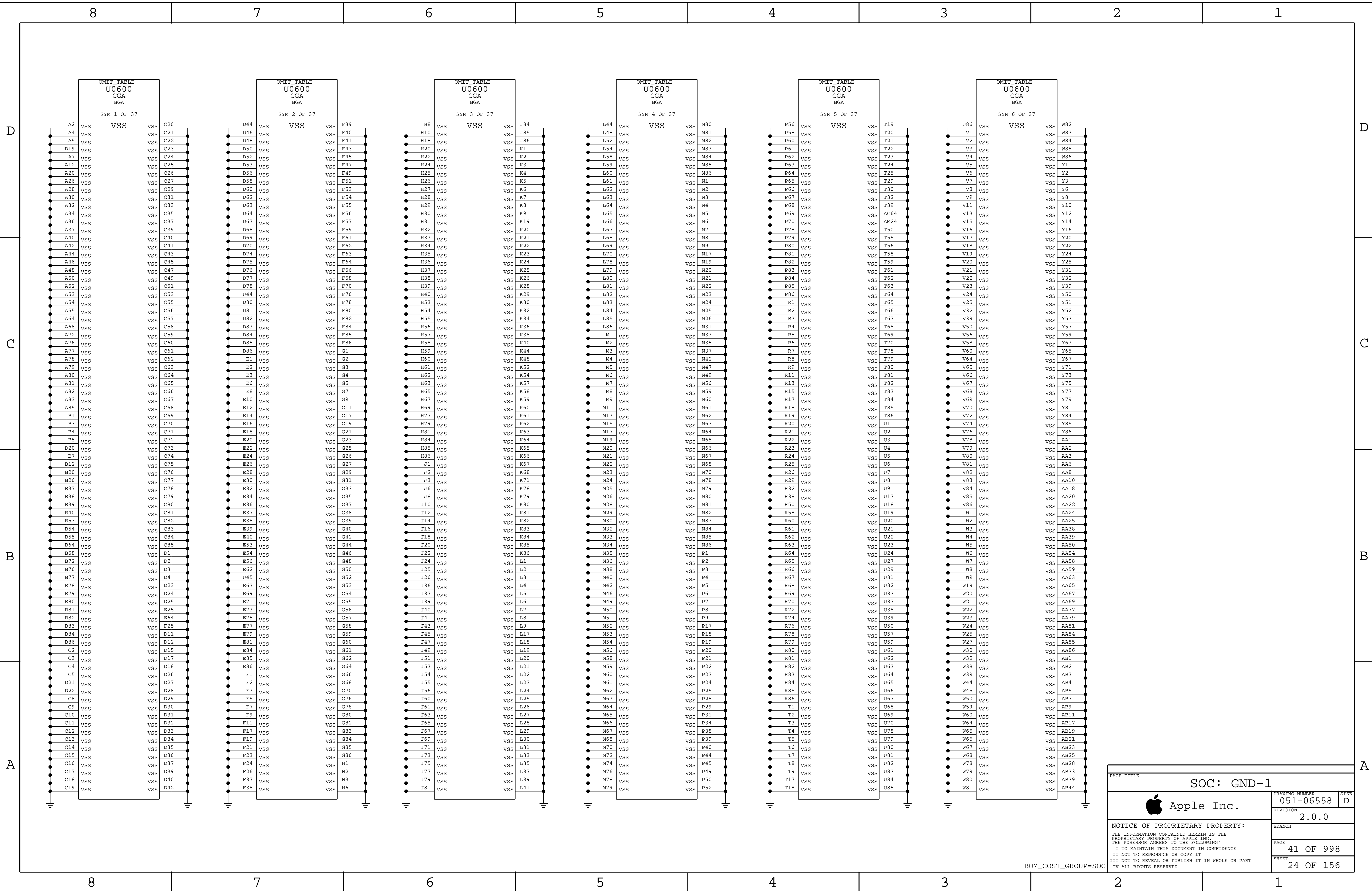








PAGE TITLE		
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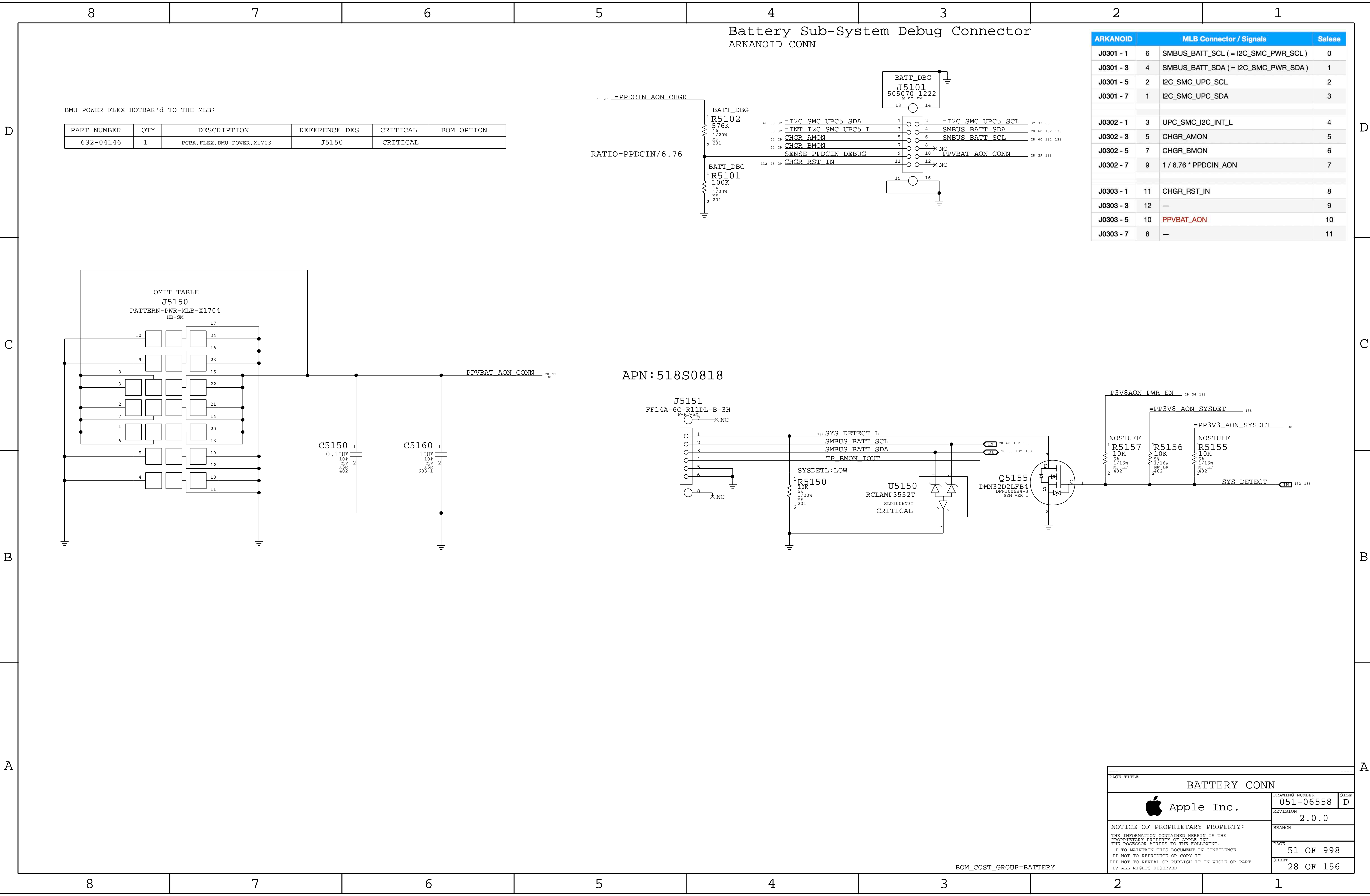
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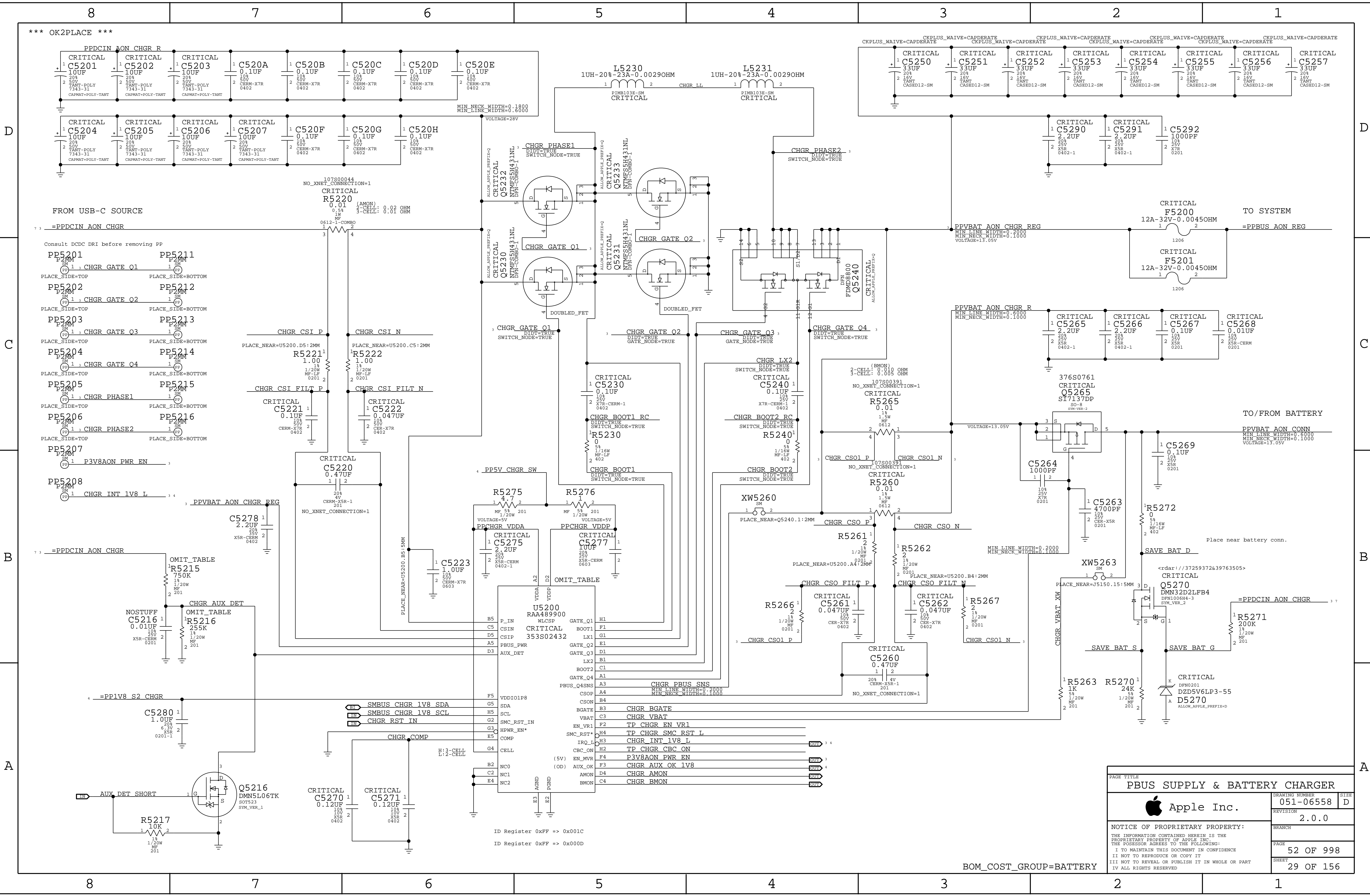



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BATTERY CONN		
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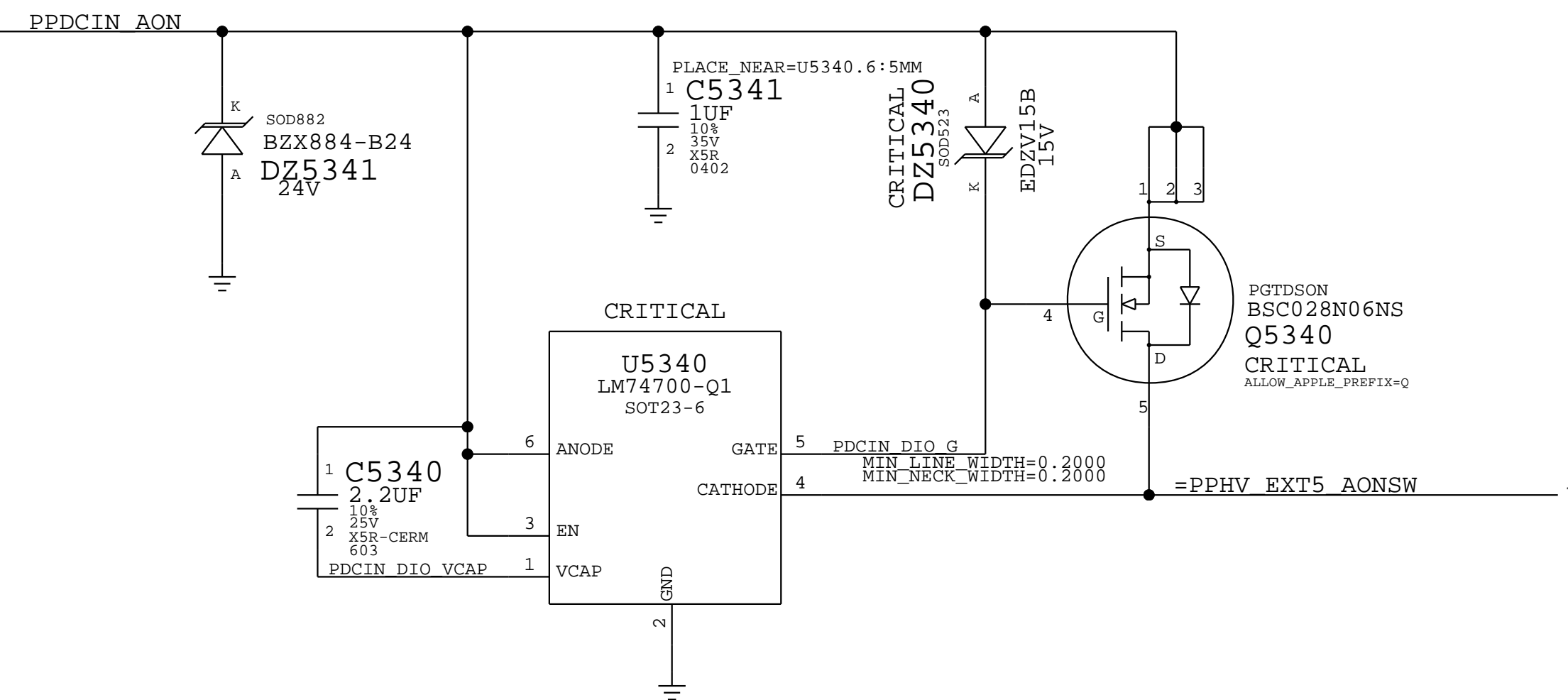
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PBUS SUPPLY & BATTERY CHARGER		
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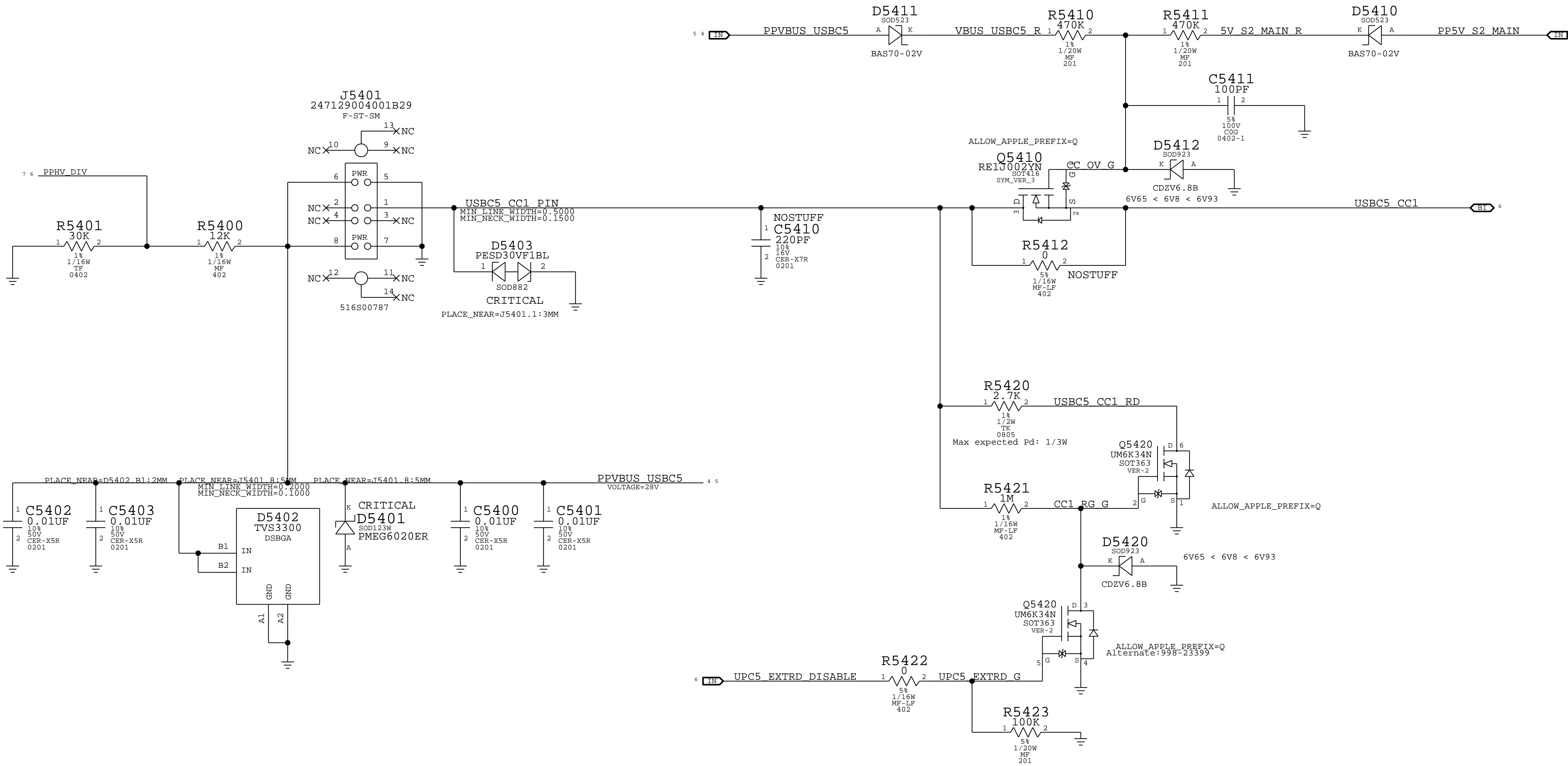
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PAGE TITLE		MAGSAFE: WHAMOLA SUPPORT	
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** OK2PLACE **


MAGSAFE MLB connector, CC OV and External RD

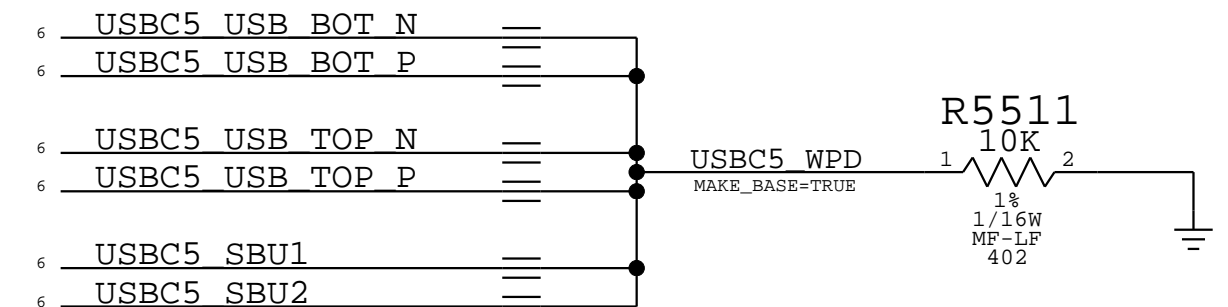
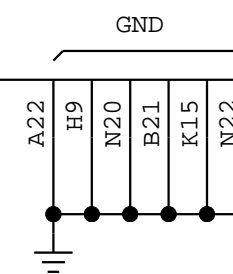
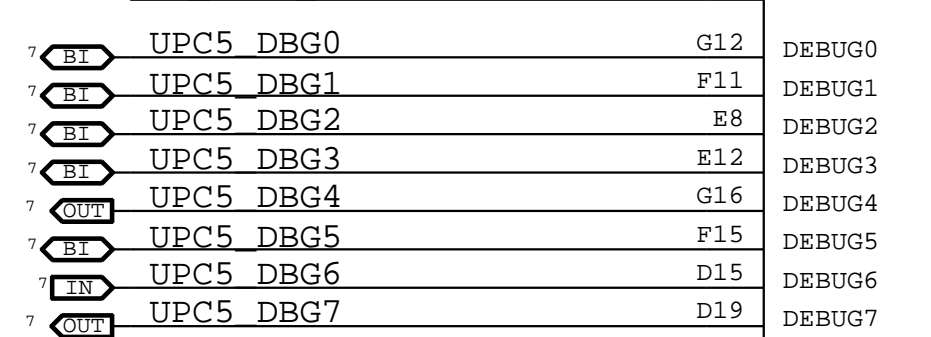
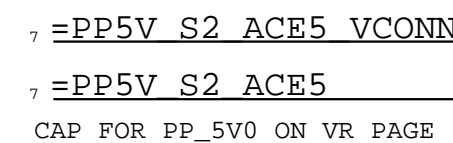
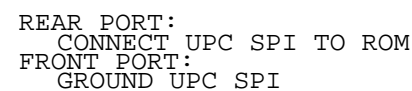
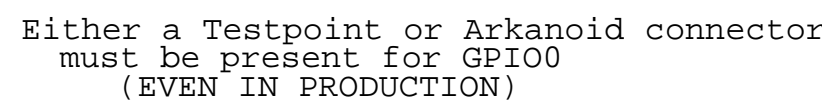



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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118S0236	1	UVLO set RL=255K	R5216	CRITICAL	SUONA_UVLO
118S0526	1	UVLO set RH=787K	R5215	CRITICAL	WHAMOLA_UVLO
118S0116	1	UVLO set RL=158K	R5216	CRITICAL	WHAMOLA_UVLO
353S02633	1	IC,RAA489900,PMIC,WHAMOLA,OTP-2,MCSF40	U5200	CRITICAL	WHAMOLA:0A5
998-24254	1	IC,RAA489900,PMIC,WHAMOLA,OTP-3,MCSF40	U5200	CRITICAL	WHAMOLA:1A

POR
PROTO BUILDS

BOM_COST_GROUP=MAGSAFE

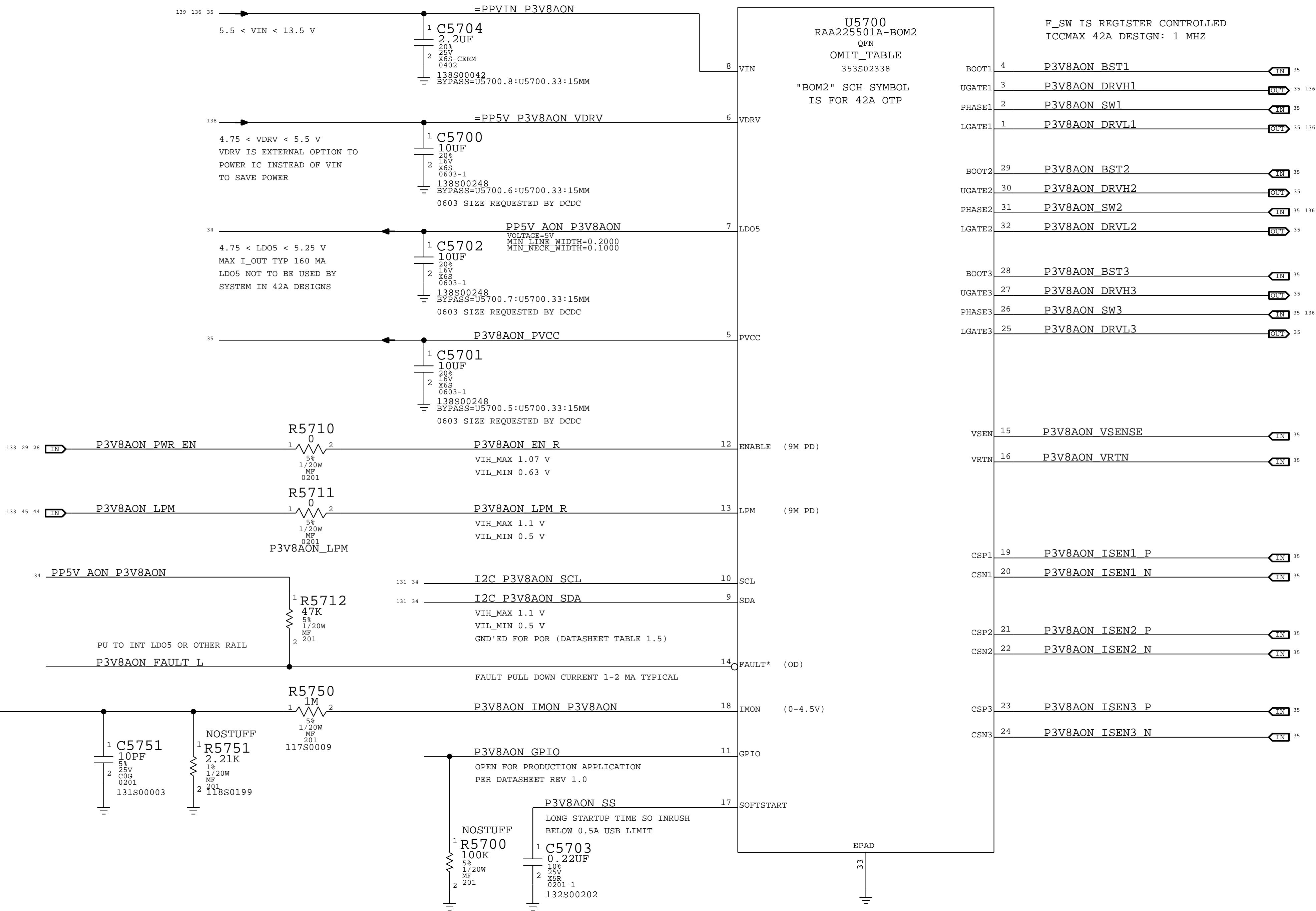
PAGE TITLE		
MAGSAFE: CONNECTOR		
 Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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	PAGE	54 OF 998
	SHEET	31 OF 156



PAGE TITLE			
MAGSAFE : PORT CONTROLLER			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-06558		D
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			2.0.0
	BRANCH		
	PAGE		
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	SHEET		
	32 OF 156		


*** OK2INTEGRATE ***

3V8 AON CONTROLLER
42A DESIGN



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02662	1	IC:RAA225501B,IC:R0M2,A2,OTP-R0C1,QP932	U5700	CRITICAL	P3V8AON_IC:A2_BOM2_R0C1
353S02604	1	IC:RAA225501B,IC:R0M2,A2,OTP-R0C0,QP932	U5700	CRITICAL	P3V8AON_IC:A2_BOM2_R0C0
353S02473	1	IC:RAA225501C,IC:R0M2,A1,OTP-R0C0,QP932	U5700	CRITICAL	P3V8AON_IC:A1_BOM2_R0C0

BOM_COST_GROUP=SOC POWER

PAGE TITLE		
POWER: 3V8 AON (1/2)		
 Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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	PAGE	57 OF 998
	SHEET	34 OF 156

42A DESIGN

D

D

C

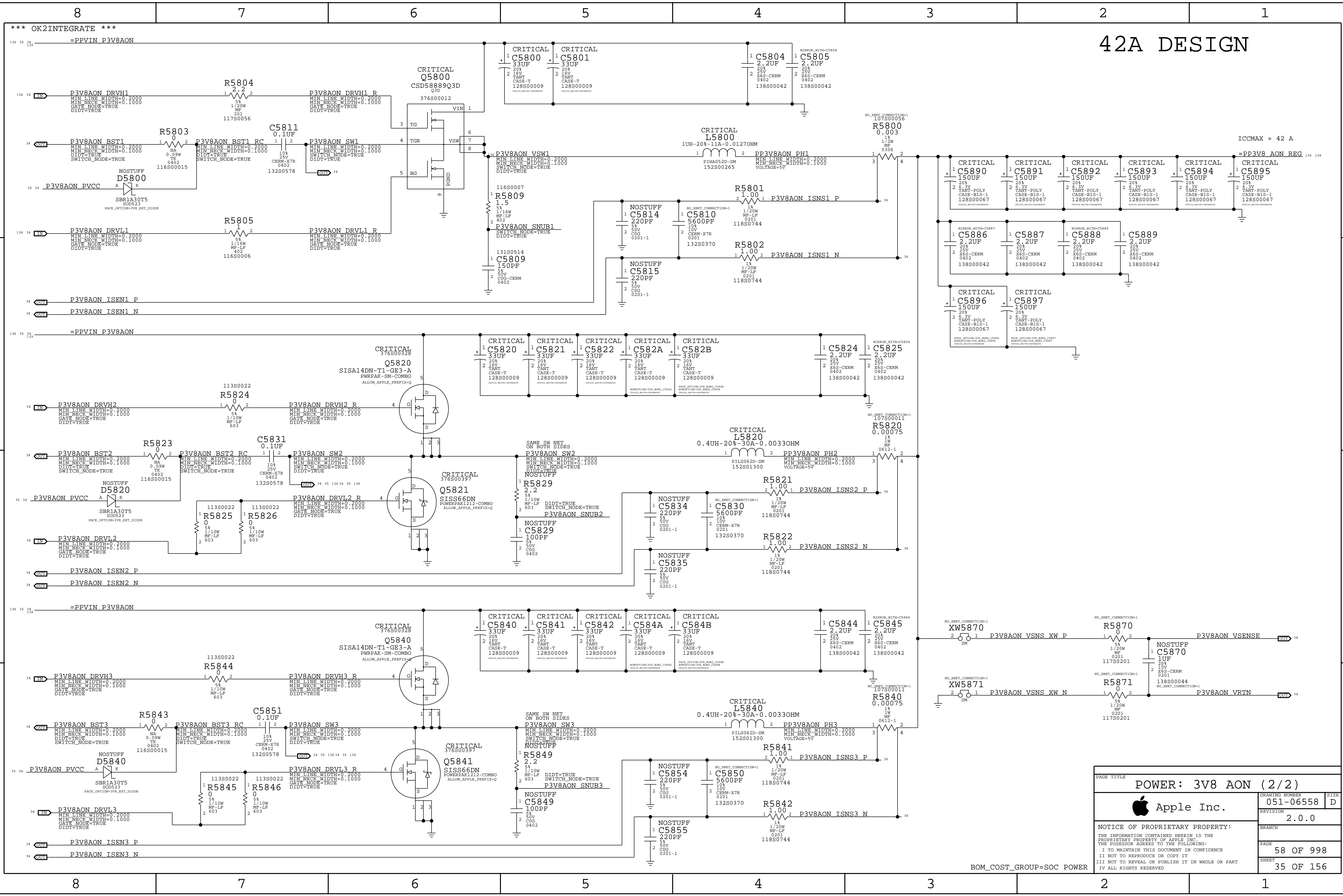
C

B

B

A

A

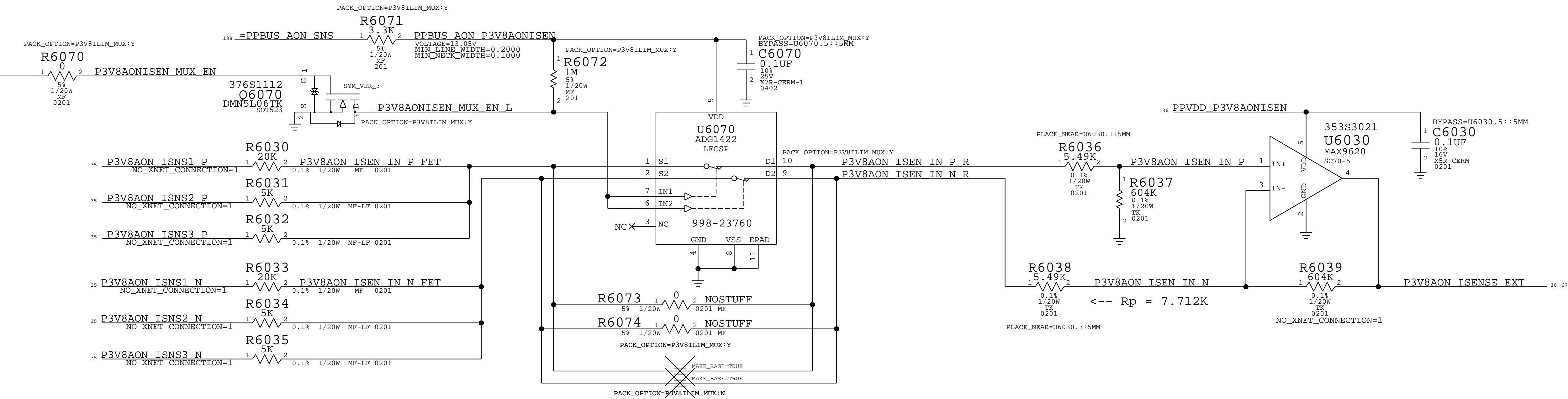


BOM_COST_GROUP=SOC POWER

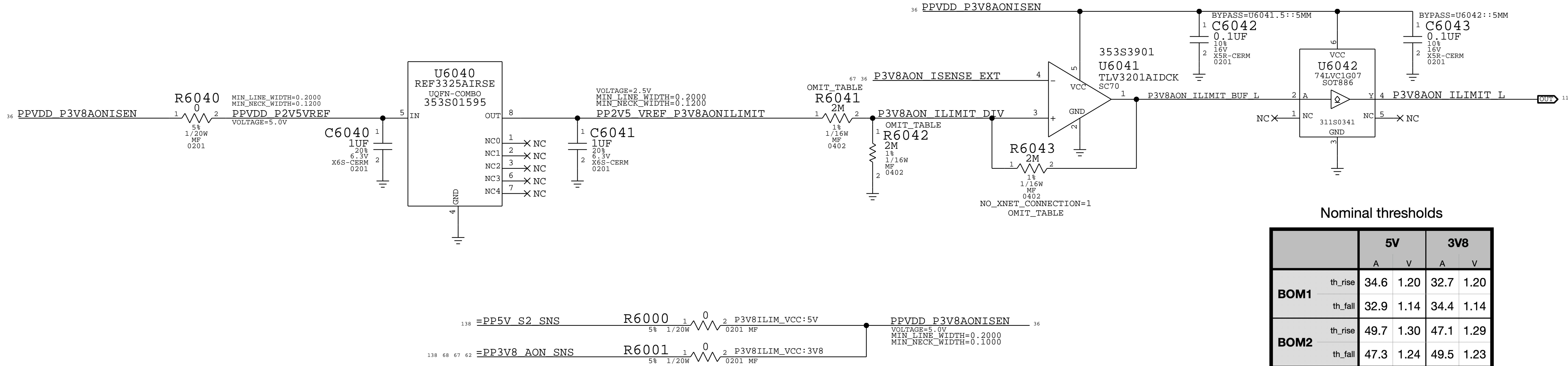
P3V8 LOW SIDE ISENSE AND ILIMIT (SUMMING AMP FOR 3 PHASES)

rdar://problem/69466996 Iceman Throttle Design Data

10A MAX ON PHASE 1, MAX TOTAL CURRENT SENSE @ PMU= 43.11A



PHASE 1 VSENSE GAIN: 8.75
PHASE 2/3 VSENSE GAIN: 35
4:1 WEIGHT FOR PHASE 1 RTREE



Nominal thresholds

		5V		3V8	
		A	V	A	V
BOM1	th_rise	34.6	1.20	32.7	1.20
	th_fall	32.9	1.14	34.4	1.14
BOM2	th_rise	49.7	1.30	47.1	1.29
	th_fall	47.3	1.24	49.5	1.23

Call one of these BOM GROUPs in the main BOM:

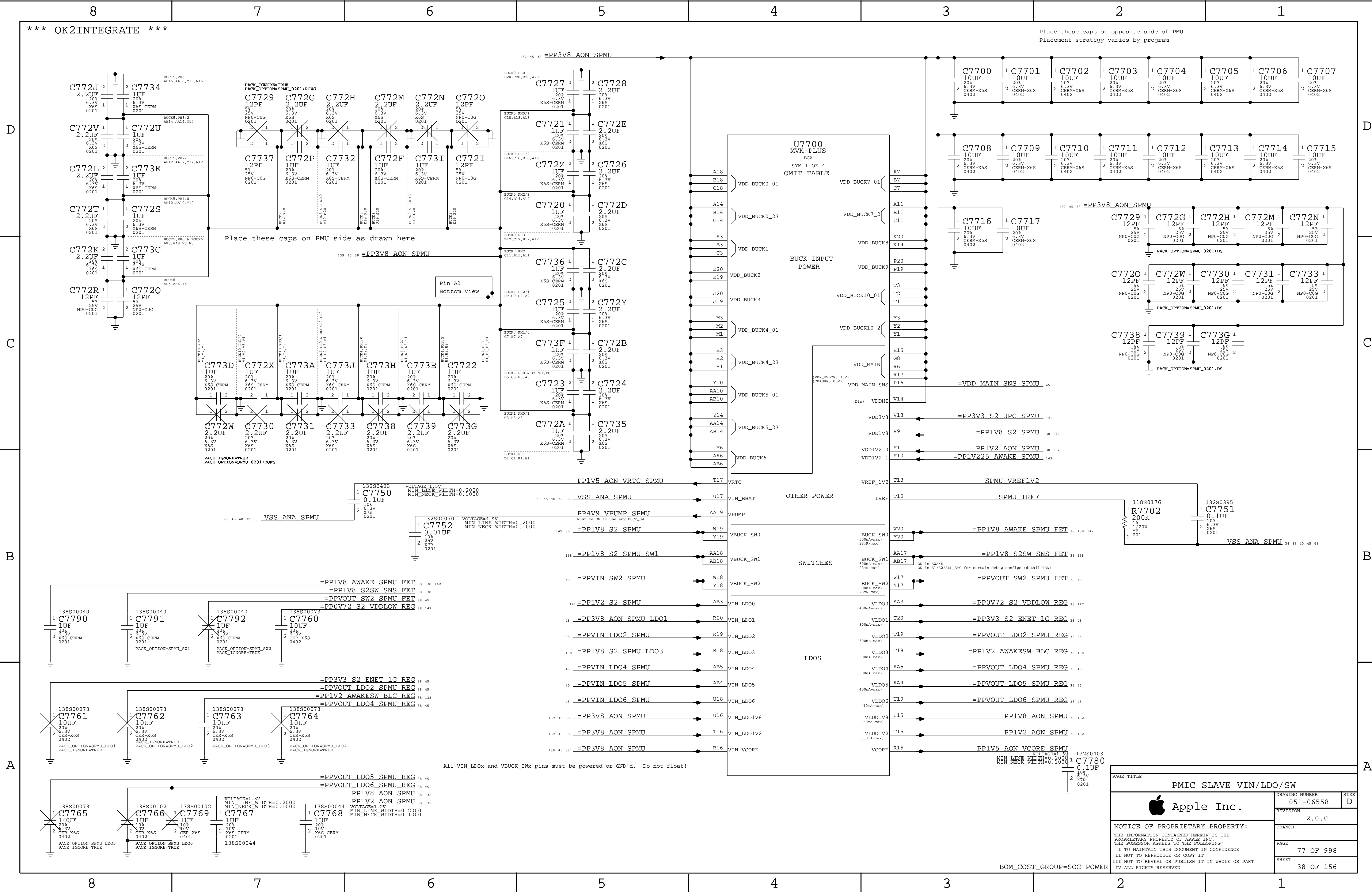
BOM GROUP	BOM OPTIONS
P3V8ILIM:BOM1_5V	P3V8ILIM_RT:23K2,P3V8ILIM_RB:20K,P3V8ILIM_RF:909K,P3V8ILIM_VCC:5V
P3V8ILIM:BOM2_5V	P3V8ILIM_RT:22K,P3V8ILIM_RB:22K,P3V8ILIM_RF:887K,P3V8ILIM_VCC:5V
P3V8ILIM:BOM1_3V8	P3V8ILIM_RT:23K2,P3V8ILIM_RB:20K,P3V8ILIM_RF:680K,P3V8ILIM_VCC:3V8
P3V8ILIM:BOM2_3V8	P3V8ILIM_RT:22K,P3V8ILIM_RB:22K,P3V8ILIM_RF:649K,P3V8ILIM_VCC:3V8

Don't Call these OPTIONs directly:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0349	1	RES,0402,1%,1/16W,23.2K	R6041	P3V8ILIM_RT:23K2
114S00141	1	RES,0402,1%,1/16W,22K	R6041	P3V8ILIM_RT:22K
114S0343	1	RES,0402,1%,1/16W,20K	R6042	P3V8ILIM_RB:20K
114S00141	1	RES,0402,1%,1/16W,22K	R6042	P3V8ILIM_RB:22K
114S0491	1	RES,0402,1%,1/16W,649K	R6043	P3V8ILIM_RF:649K
114S00146	1	RES,0402,1%,1/16W,680K	R6043	P3V8ILIM_RF:680K
114S0504	1	RES,0402,1%,1/16W,887K	R6043	P3V8ILIM_RF:887K
114S0505	1	RES,0402,1%,1/16W,909K	R6043	P3V8ILIM_RF:909K

BOM_COST_GROUP=SOC POWER

PAGE TITLE		
POWER: 3V8 AON OUTPUT THROTTLE		
	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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		PAGE
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*** OK2INTEGRATE ***

System BUCK11
Vboot = 0.775V
IOUT_MAX = 19.2A

System BUCK16
Vboot = 0.8875V
IOUT_MAX = 2.1A
OFF in SLF_SMC, and S2 if C10 is unplugged

System BUCK15
Vboot = 0.775V
IOUT_MAX = 9A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0010	1	RES, MF, 10.00HM, 1, 1/20W, 0201	R7870	CRITICAL	MAV:A0
117S0201	1	RES, MF, 1A MAX, 0.0 OHM, 5A, 0201, BLACK	R7870	CRITICAL	MAV:B0

PACK_OPTION=PMU_DISP2:Y

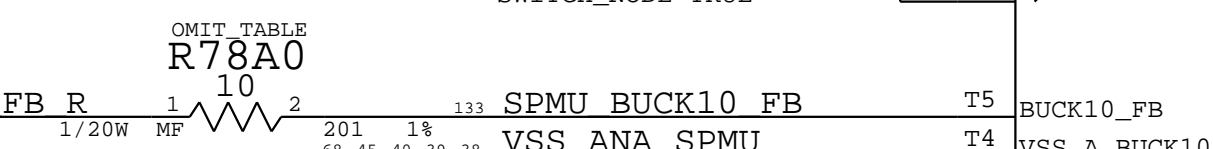
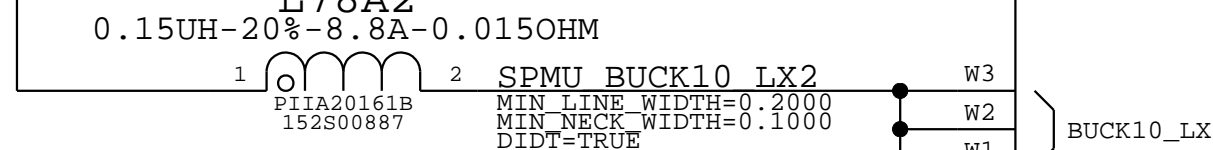
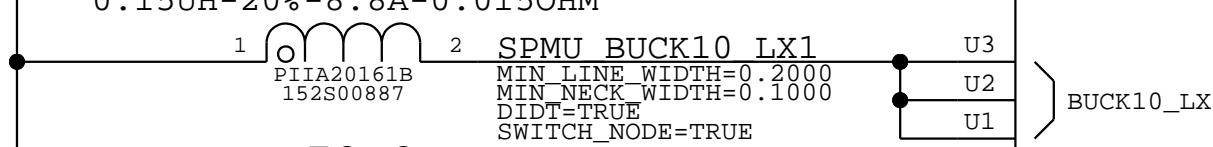
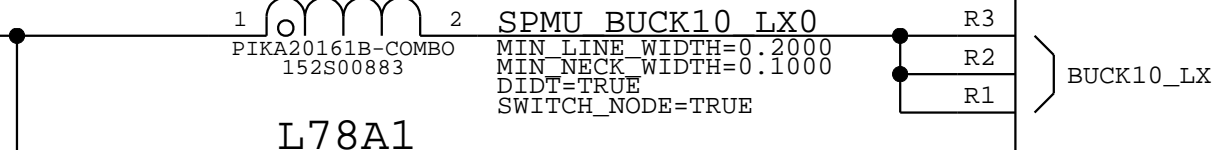
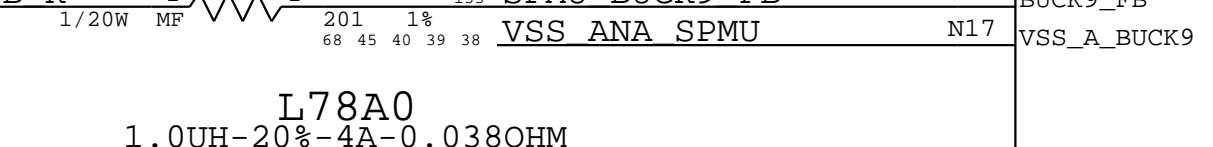
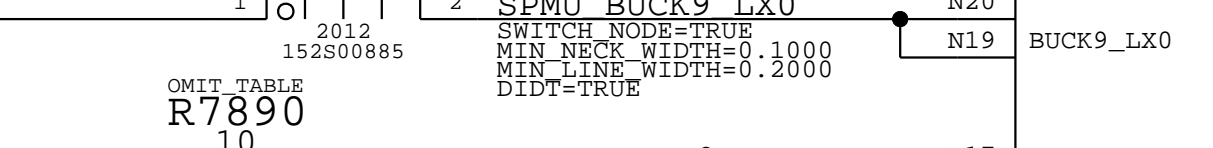
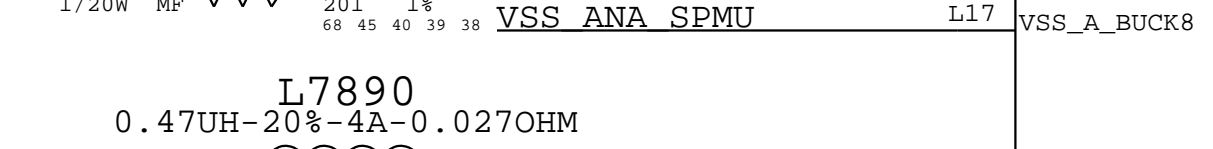
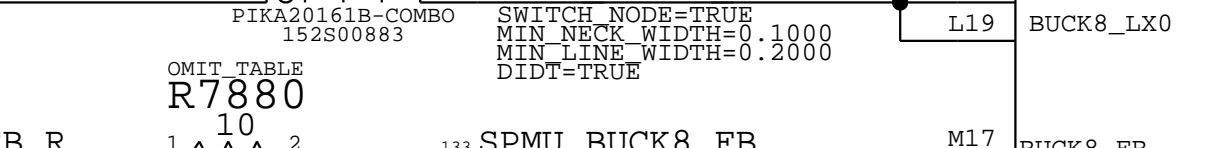
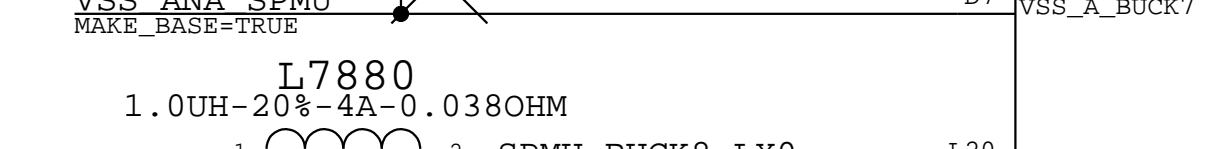
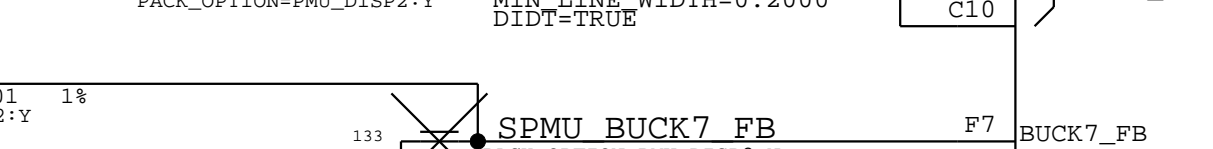
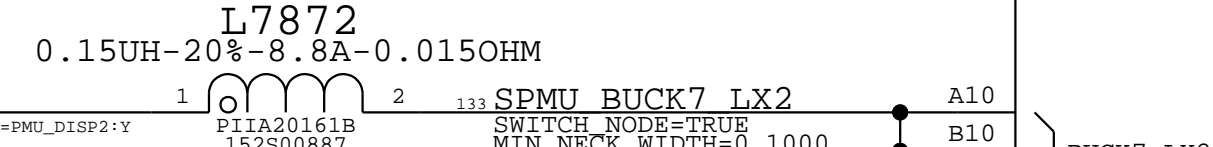
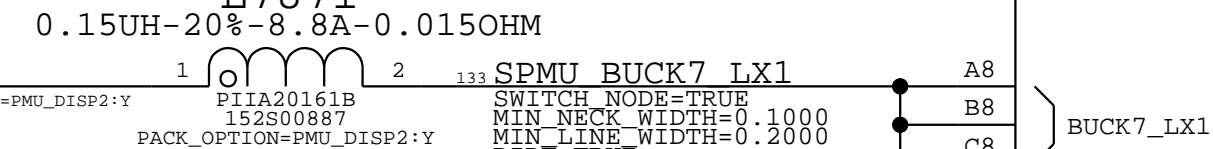
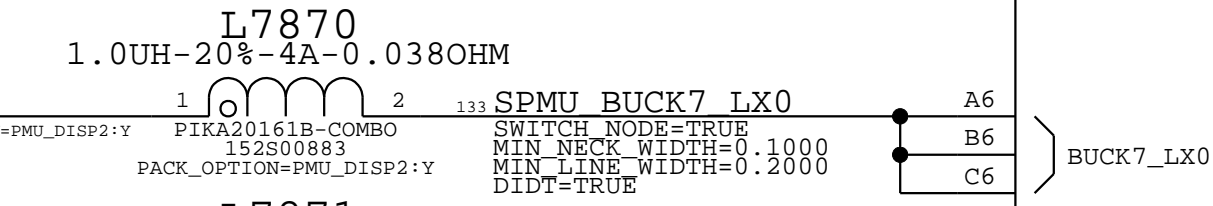
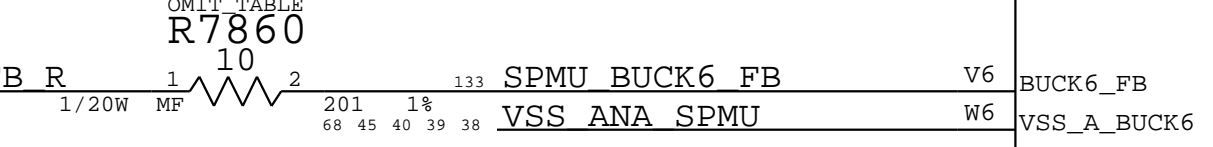
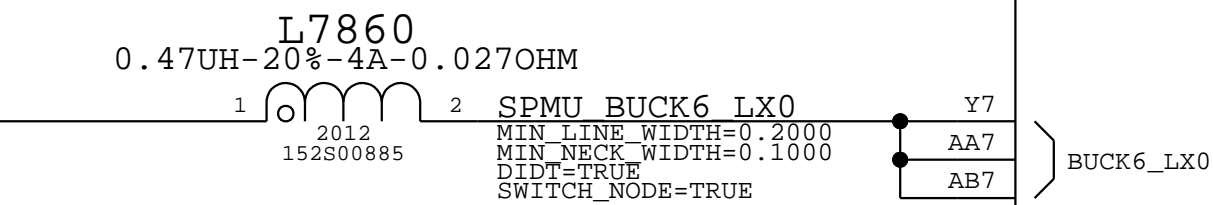
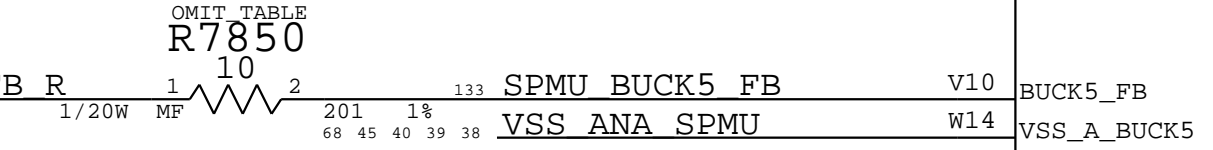
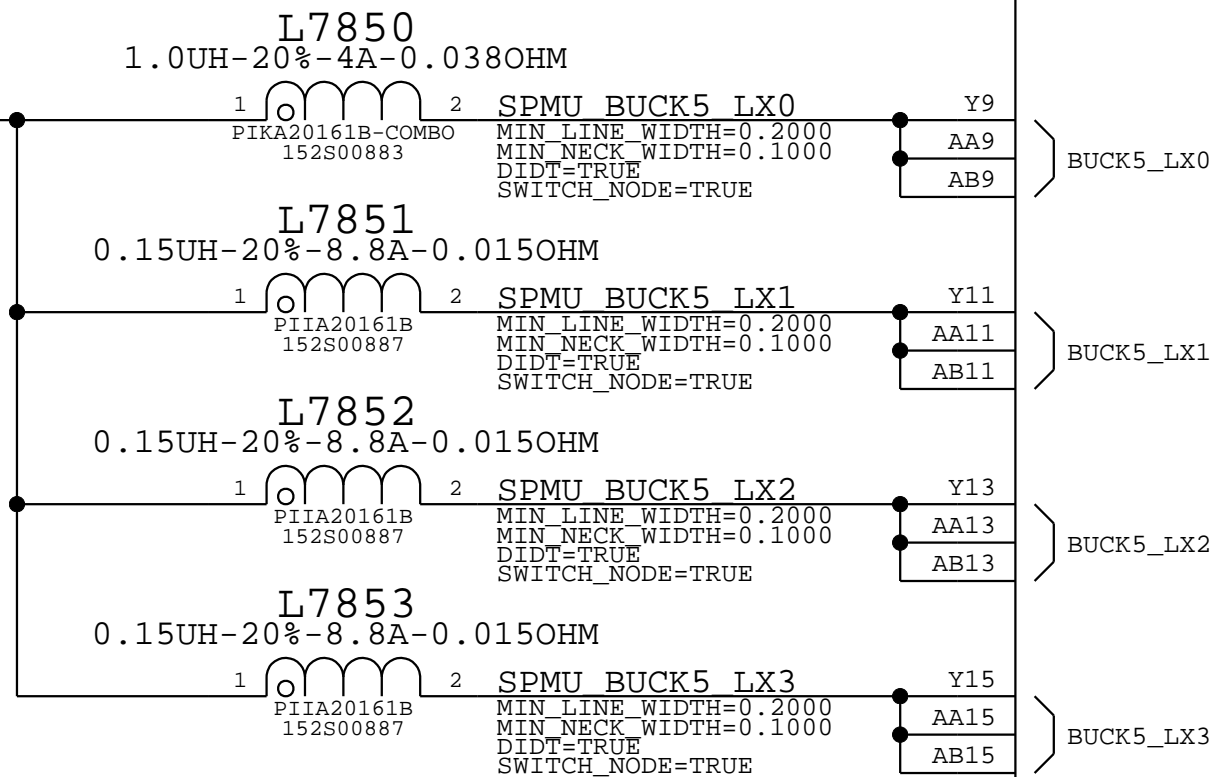
System BUCK12
Vboot = 1.225V
IOUT_MAX = 3.2A

System BUCK21
Vboot = 1.12188V
IOUT_MAX = 2.1A
OFF in SLF_SMC

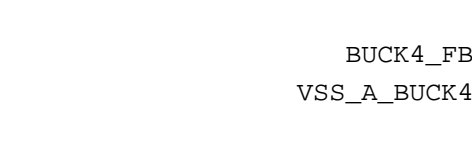
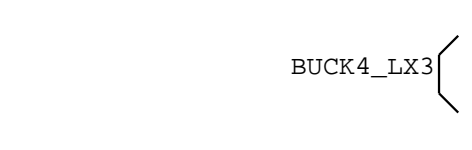
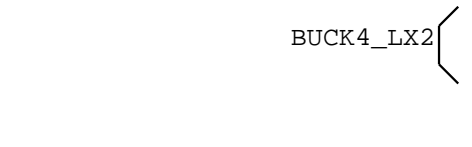
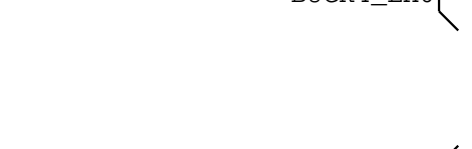
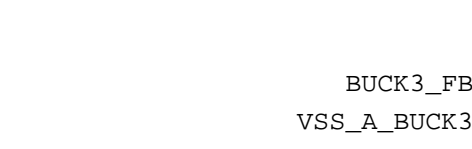
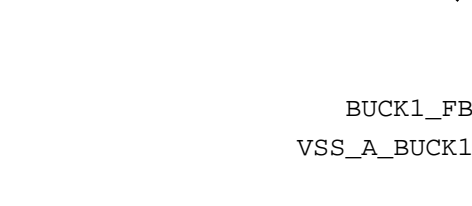
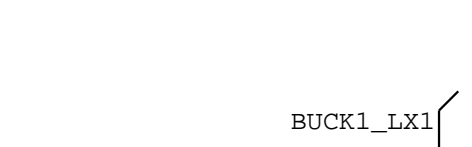
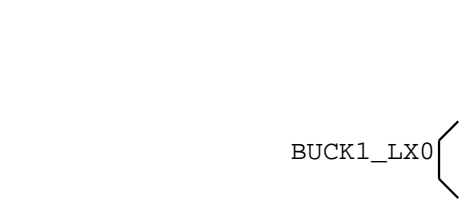
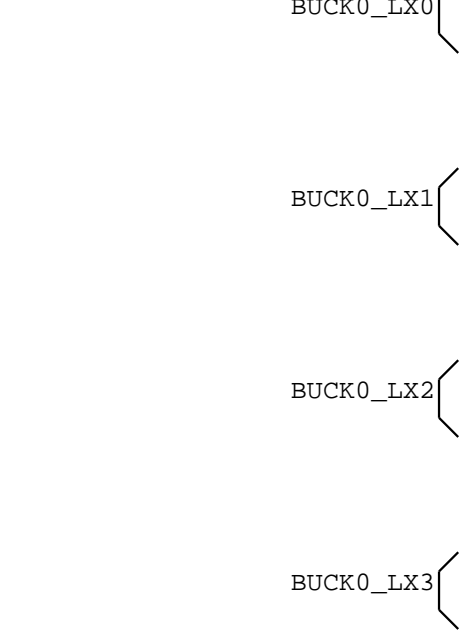
System BUCK20
Vboot = 0.775V
Iout_Max = 13.2A/14.3A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0010	5	RES, MF, 10.00HM, 1, 1/20W, 0201	RT850, RT852, RT853, RT854	CRITICAL	MAV:A0
117S0201	5	RES, MF, 1A MAX, 0.0 OHM, 5A, 0201, BLACK	RT850, RT852, RT853, RT854	CRITICAL	MAV:B0
118S0010	5	RES, MF, 10.00HM, 1, 1/20W, 0201	RT850, RT852, RT853, RT854	CRITICAL	MAV:A0
117S0201	5	RES, MF, 1A MAX, 0.0 OHM, 5A, 0201, BLACK	RT850, RT852, RT853, RT854	CRITICAL	MAV:B0

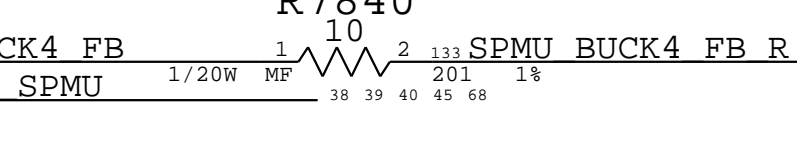
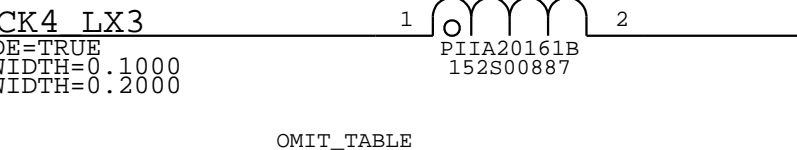
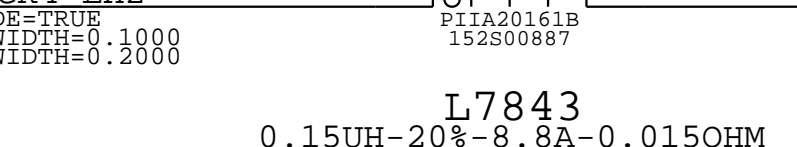
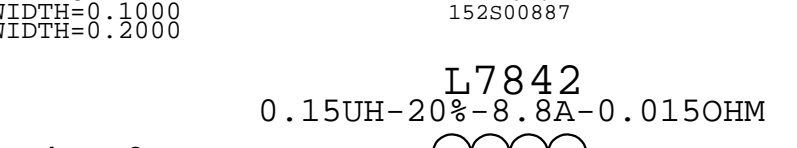
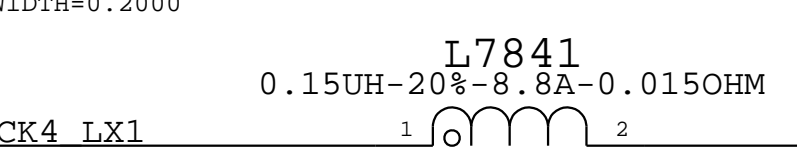
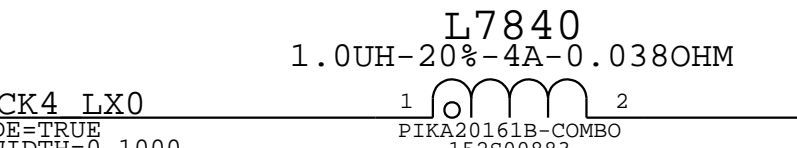
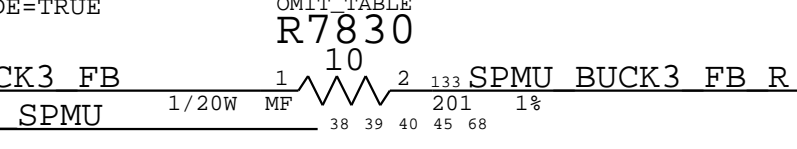
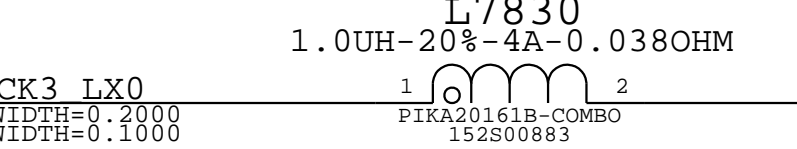
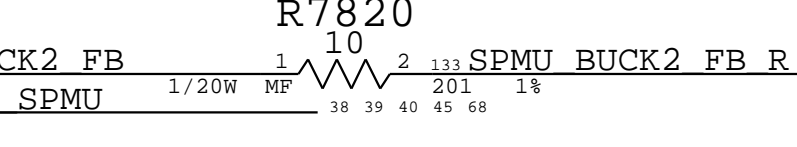
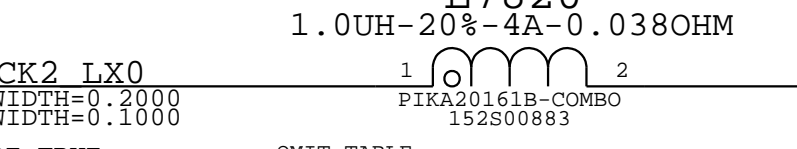
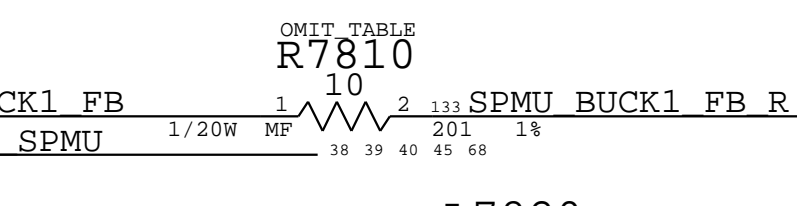
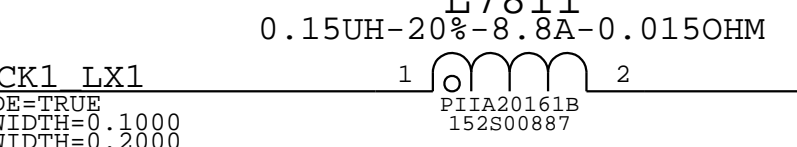
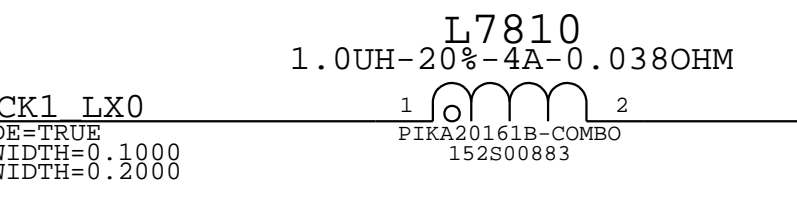
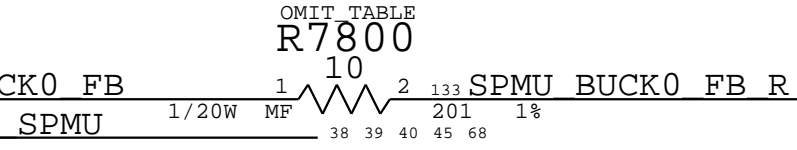
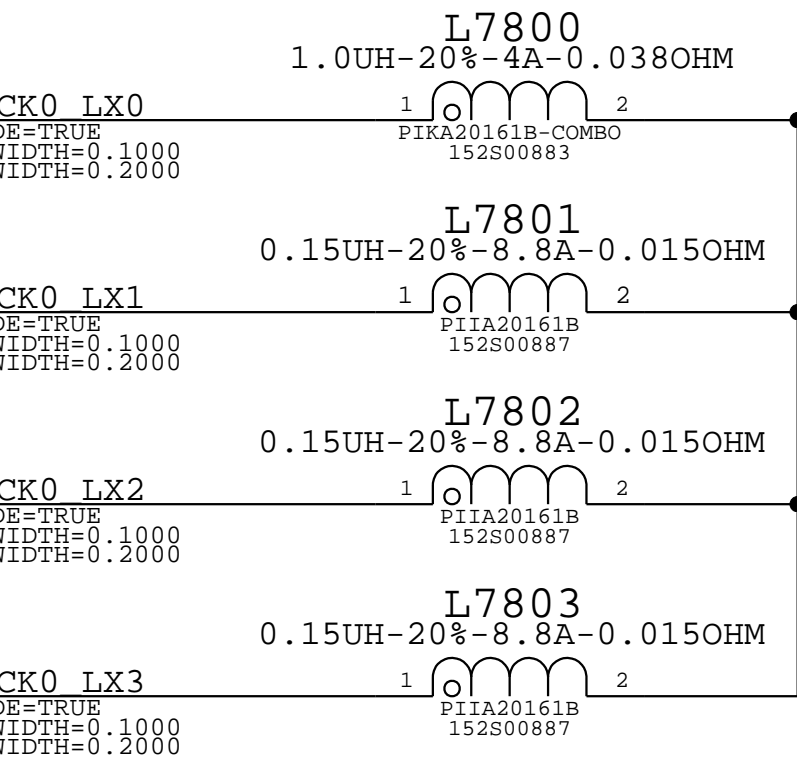
SLAVE BUCKS



U7700
MVK-PLUS
BGA
SYM 2 OF 4
OMIT_TABLE



TOD0: XW's are only for 16L boards. TBD how to manage this in a ref-schematic



System BUCK17
Vboot = 0.7V
IOUT_MAX = 19.2A

System BUCK13
Vboot = 0.575V
IOUT_MAX = 5.4A

System BUCK18
Vboot = 0.9V
IOUT_MAX = 3.2A
OFF in SLF_SMC

System BUCK19
Vboot = 1.8V
IOUT_MAX = 3.4A

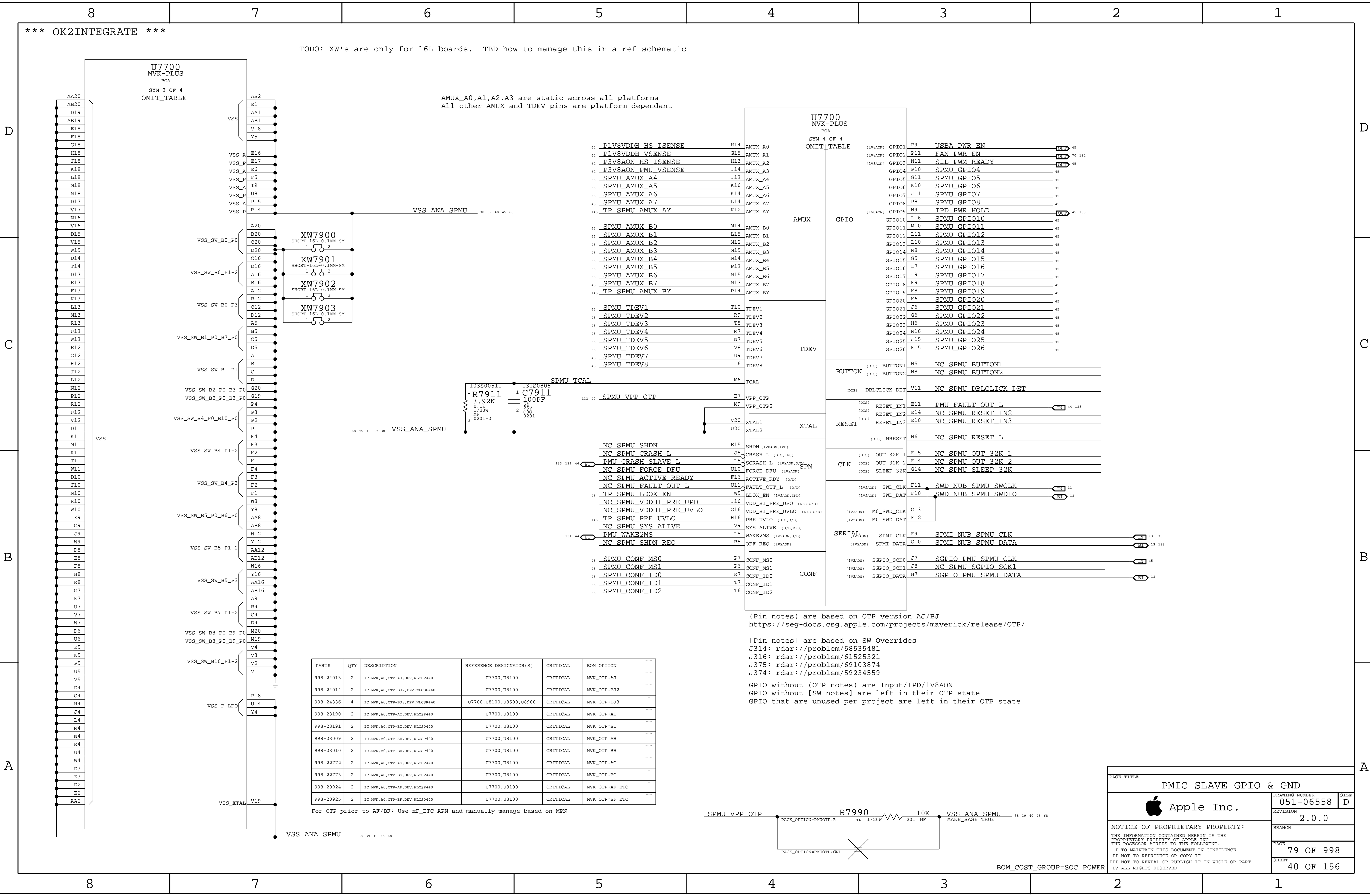
System BUCK14
Vboot = 1.1V
IOUT_MAX = 15A
OFF in SLF_SMC

PAGE TITLE		
PMIC SLAVE BUCKS		
Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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Iout-max is based on PMIC datasheet lv3

Vboot is based on AJ/BJ OTP (* indicates 0V initial boot)

BOM_COST_GROUP=SOC POWER



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-24013	2	IC,MVK,A0,OTP-AJ,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AJ
998-24014	2	IC,MVK,A0,OTP-BJ2,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BJ2
998-24336	4	IC,MVK,A0,OTP-BJ3,DEV,MLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:BJ3
998-23190	2	IC,MVK,A0,OTP-AI,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AI
998-23191	2	IC,MVK,A0,OTP-BI,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BI
998-23009	2	IC,MVK,A0,OTP-AH,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AH
998-23010	2	IC,MVK,A0,OTP-BH,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BH
998-22772	2	IC,MVK,A0,OTP-AG,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AG
998-22773	2	IC,MVK,A0,OTP-BG,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BG
998-20924	2	IC,MVK,A0,OTP-AF,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AF_ETC
998-20925	2	IC,MVK,A0,OTP-BF,DEV,MLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BF_ETC

For OTP prior to AF/BF: Use xF_ETC APN and manually manage based on MPN

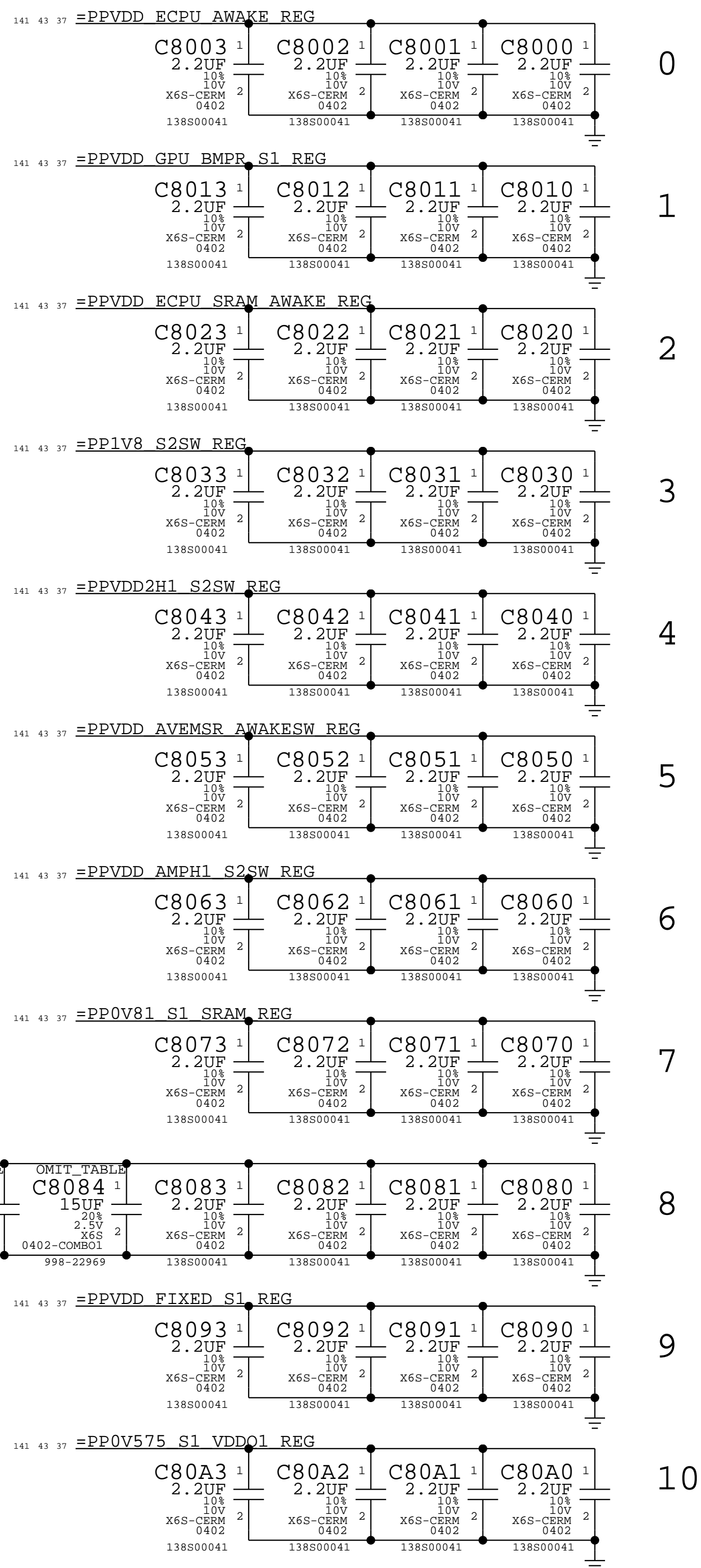
(Pin notes) are based on OTP version AJ/BJ
<https://seg-docs.csg.apple.com/projects/maverick/release/OTP/>

[Pin notes] are based on SW Overrides
J314: rdar://problem/58535481
J316: rdar://problem/61525321
J375: rdar://problem/69103874
J374: rdar://problem/59234559
GPIO without (OTP notes) are Input/IPD/1V8AON
GPIO without [SW notes] are left in their OTP state
GPIO that are unused per project are left in their OTP state

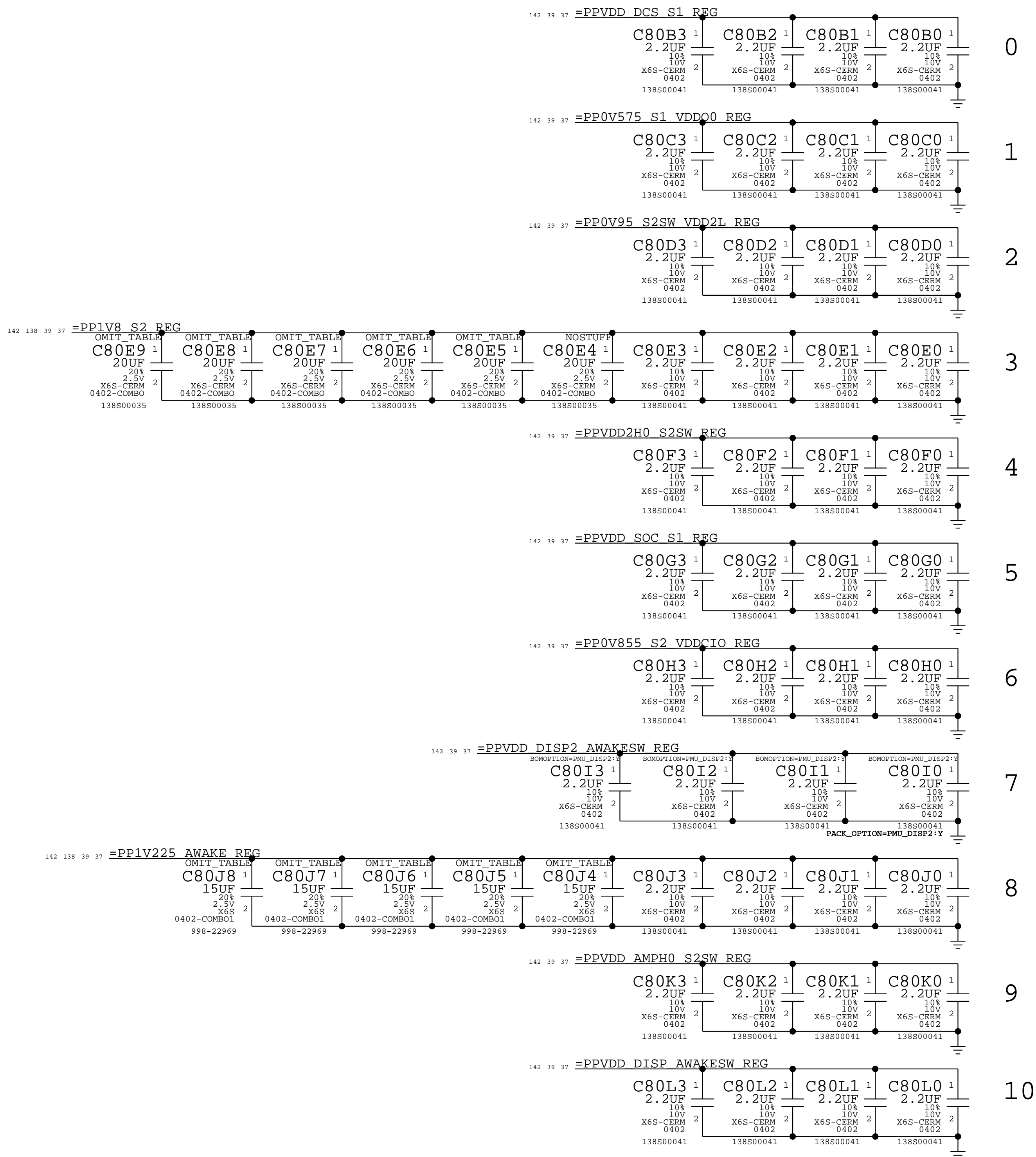
PAGE TITLE		
PMIC SLAVE GPIO & GND		
	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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	SHEET	40 OF 156

*** OK2INTEGRATE ***

MASTER



SLAVE

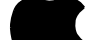


Output Desense Caps to be drawn on project-specific page(s):

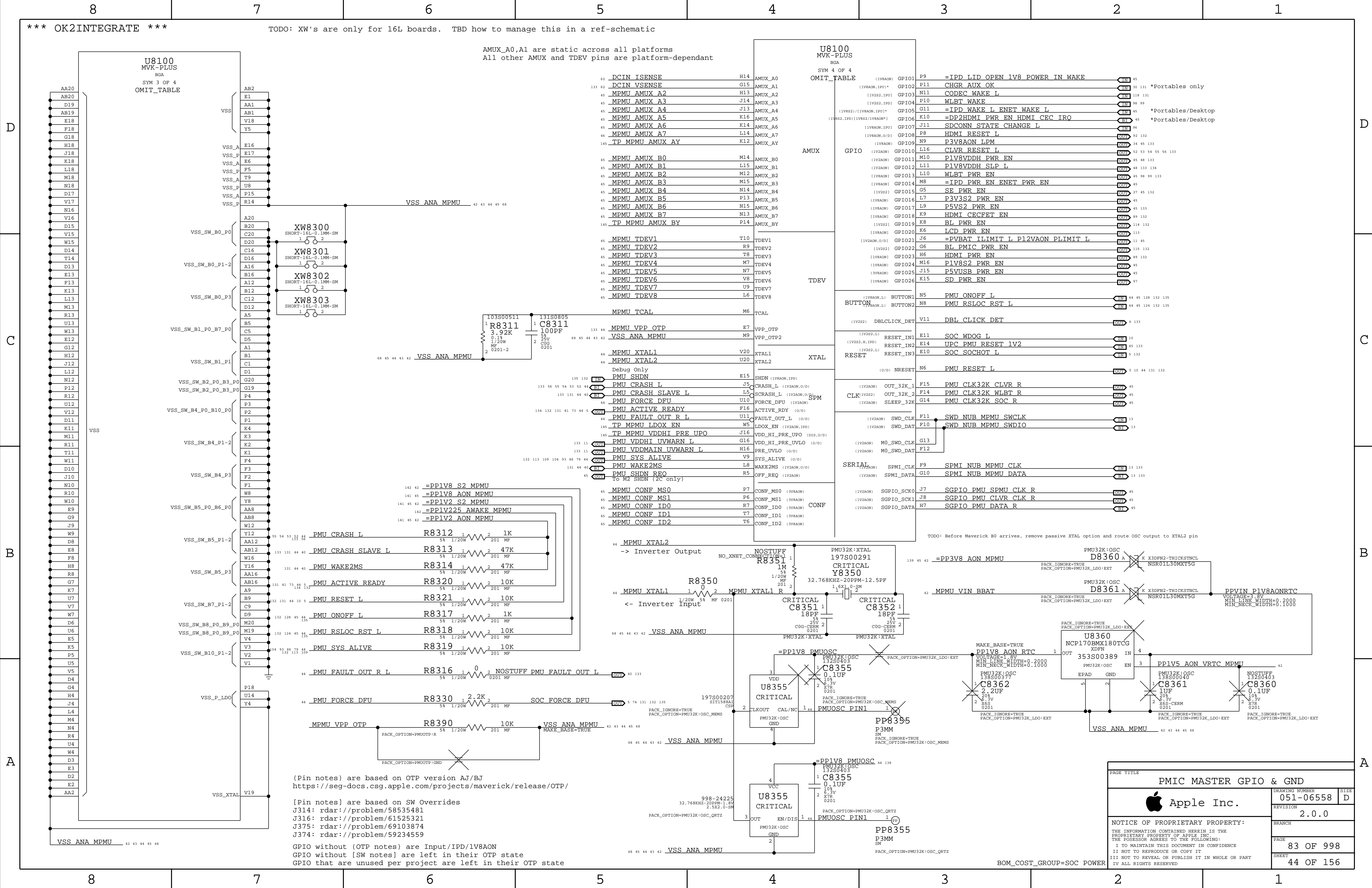
1x each 3pF+12pF for 1/2phase Buck: 1/2/3/6/8/9/10_M

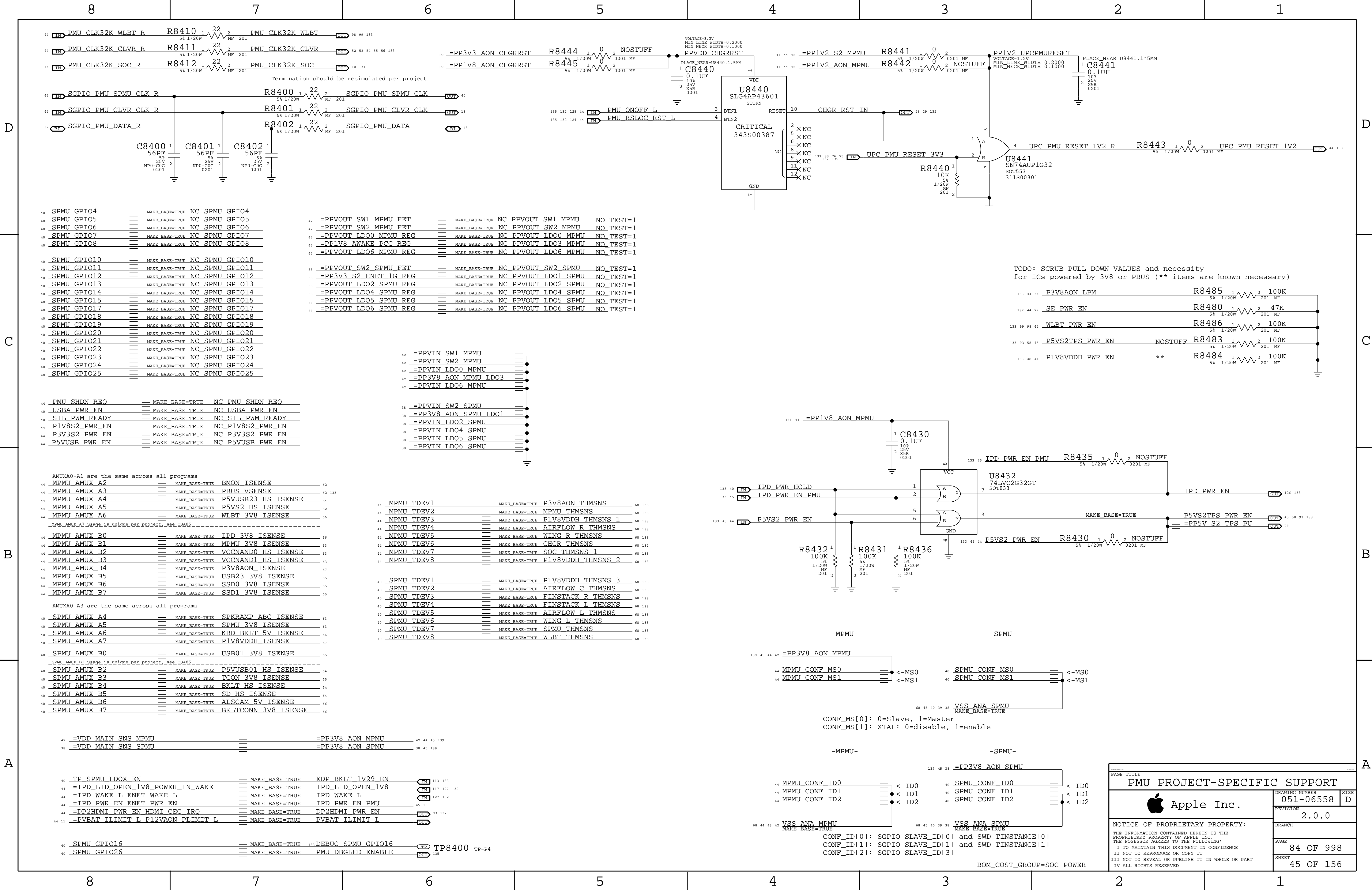
2x each 3pF+12pF for 3/4-phase Buck: 0/4/5/7/10_S

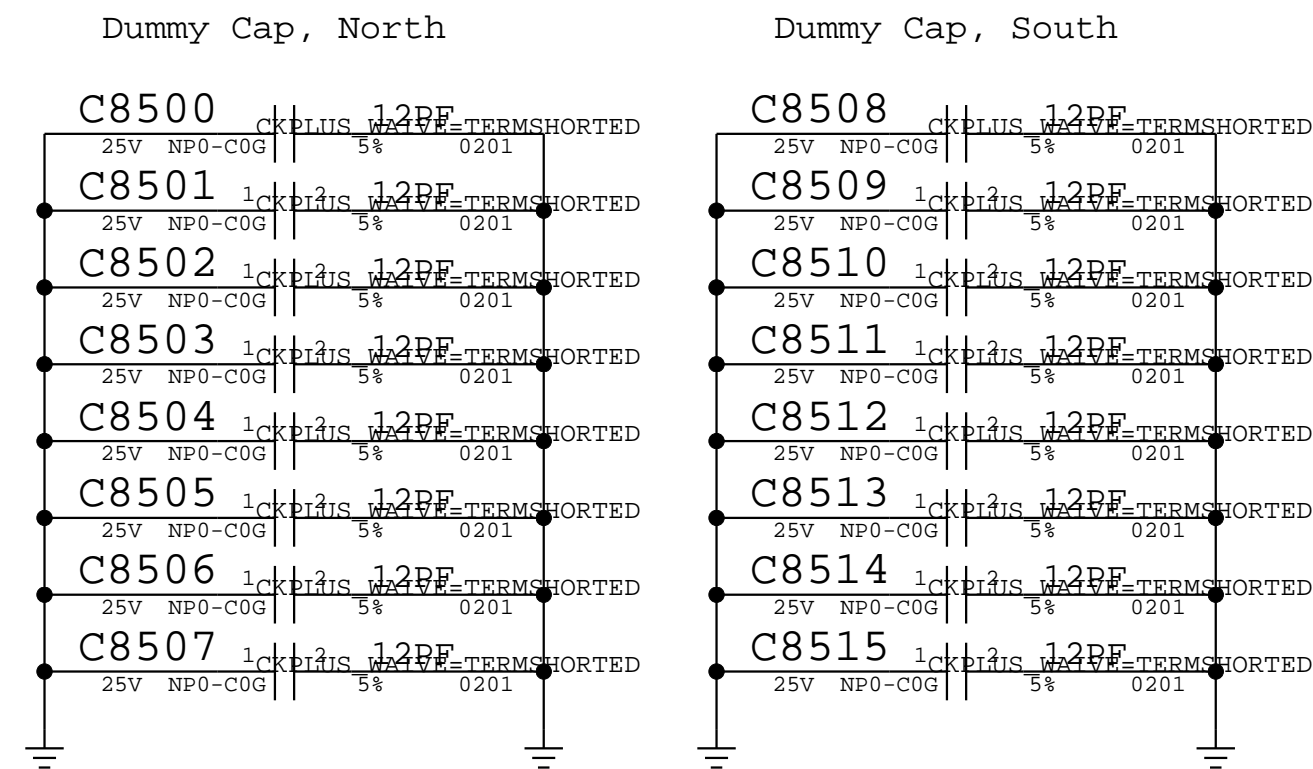
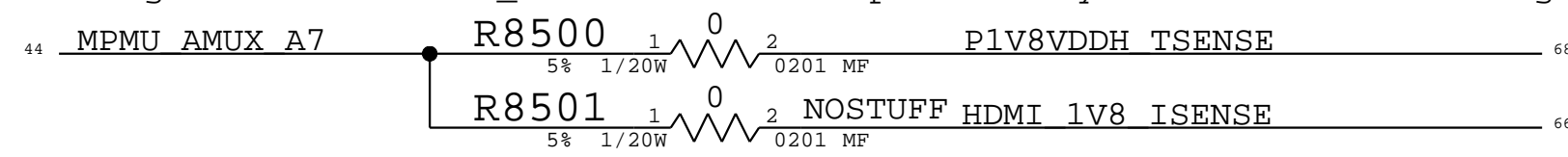
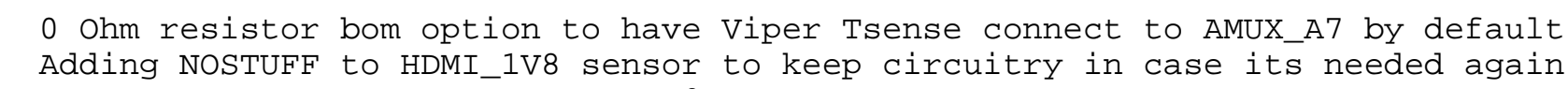
BOM_COST_GROUP=SOC POWER


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PMIC BUCK OUTPUT CAPS		051-06558		D
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		2.0.0		
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		80 OF 998		
		SHEET		
		41 OF 156		

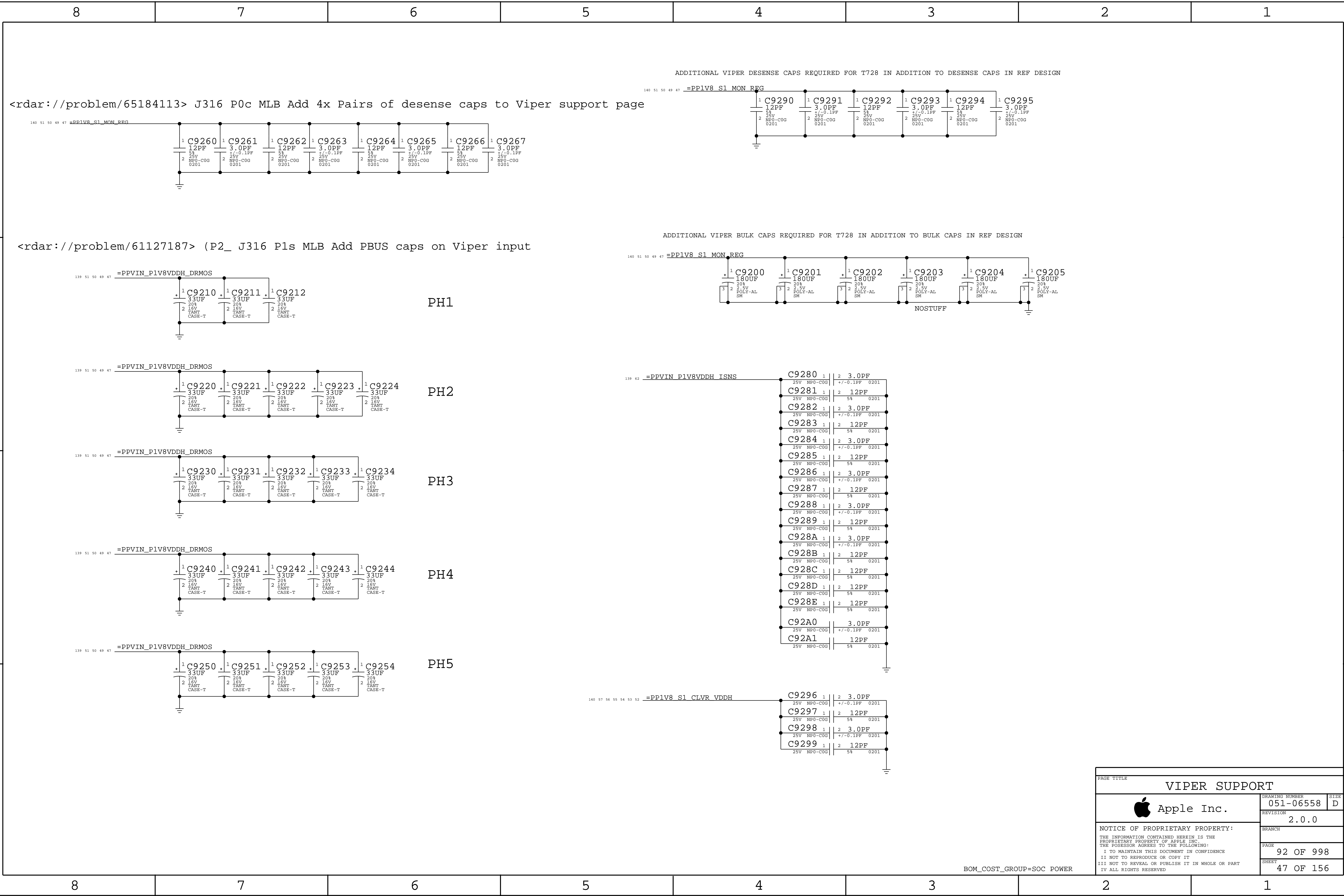








BOM_COST_GROUP=PLATFORM POWER			
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PMU PROJECT SPECIFIC SUPPORT 2			
 Apple Inc.	DRAWING NUMBER		SIZE
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		85 OF 998	
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		46 OF 156	



8

7

6

5

4

3

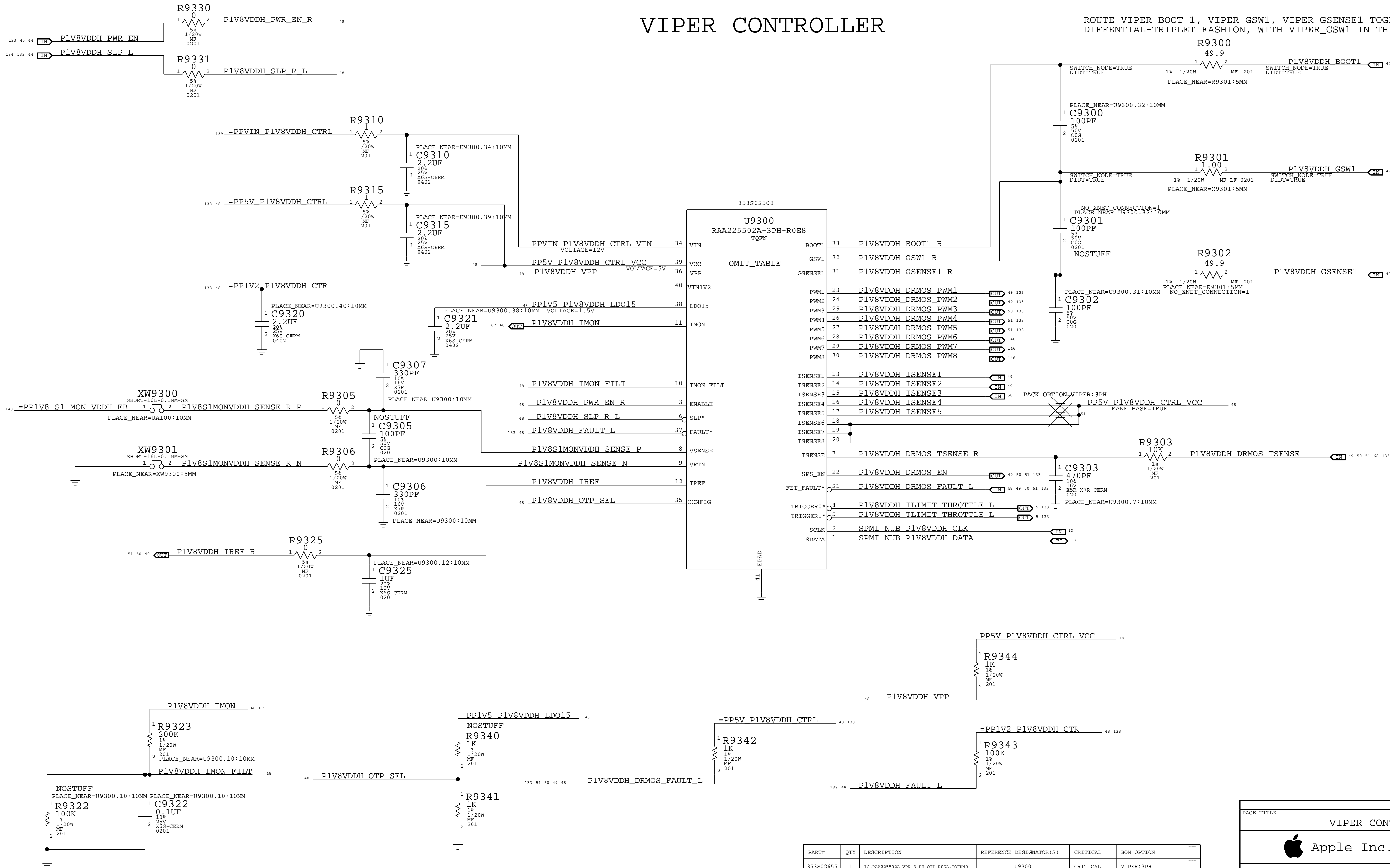
2

1

OK2INTEGRATE


VIPER CONTROLLER

ROUTE VIPER_BOOT_1, VIPER_GSW1, VIPER_GSENSE1 TOGETHER IN DIFFENTIAL-TRIPLET FASHION, WITH VIPER_GSW1 IN THE MIDDLE



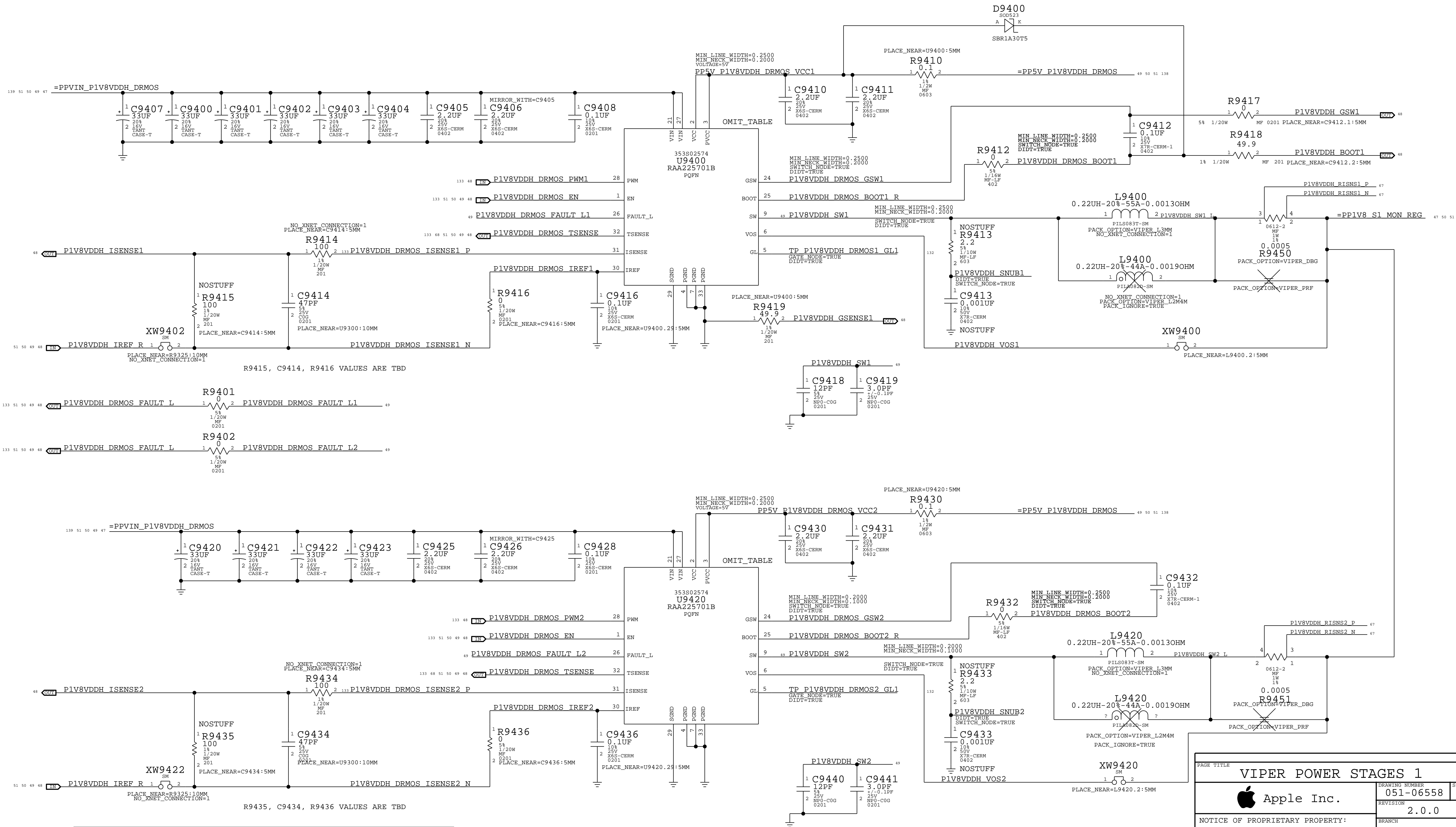
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353802655	1	IC,RAA225502A,VPR,3-PH,OTP-R0EA,TQFN40	U9300	CRITICAL	VIPER:3PH
353802353	1	IC,RAA225502A,VPR,5-PH,OTP-R0F0	U9300	CRITICAL	VIPER:5PH

BOM_COST_GROUP=SOC POWER

PAGE TITLE		
VIPER CONTROLLER		
 Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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	PAGE	93 OF 998
	SHEET	48 OF 156

OK2INTEGRATE

VIPER POWER STAGES 1



D

D



C

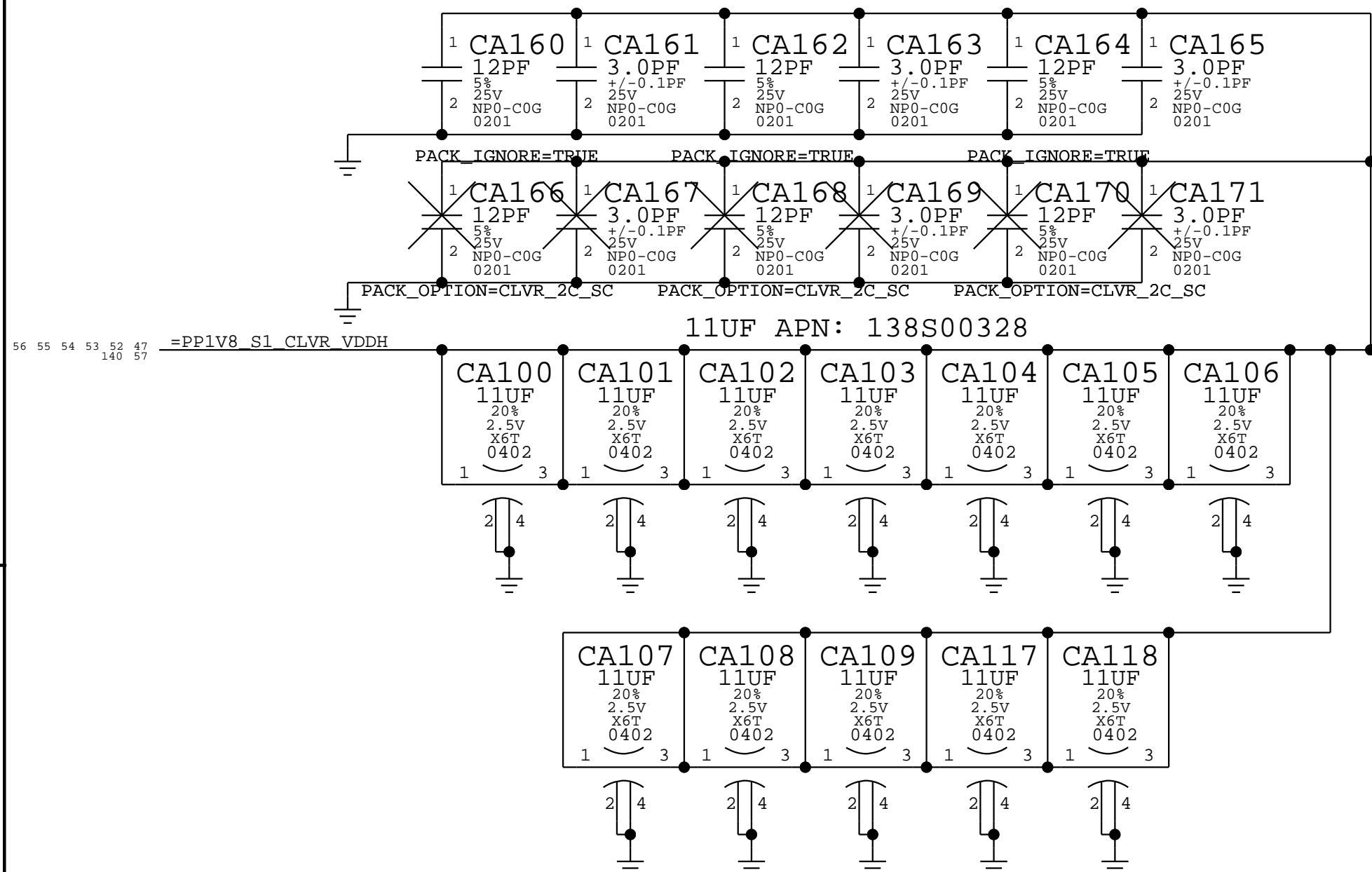
BAA

8	7	6	5	4	3	2	1
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OK2INTEGRATE

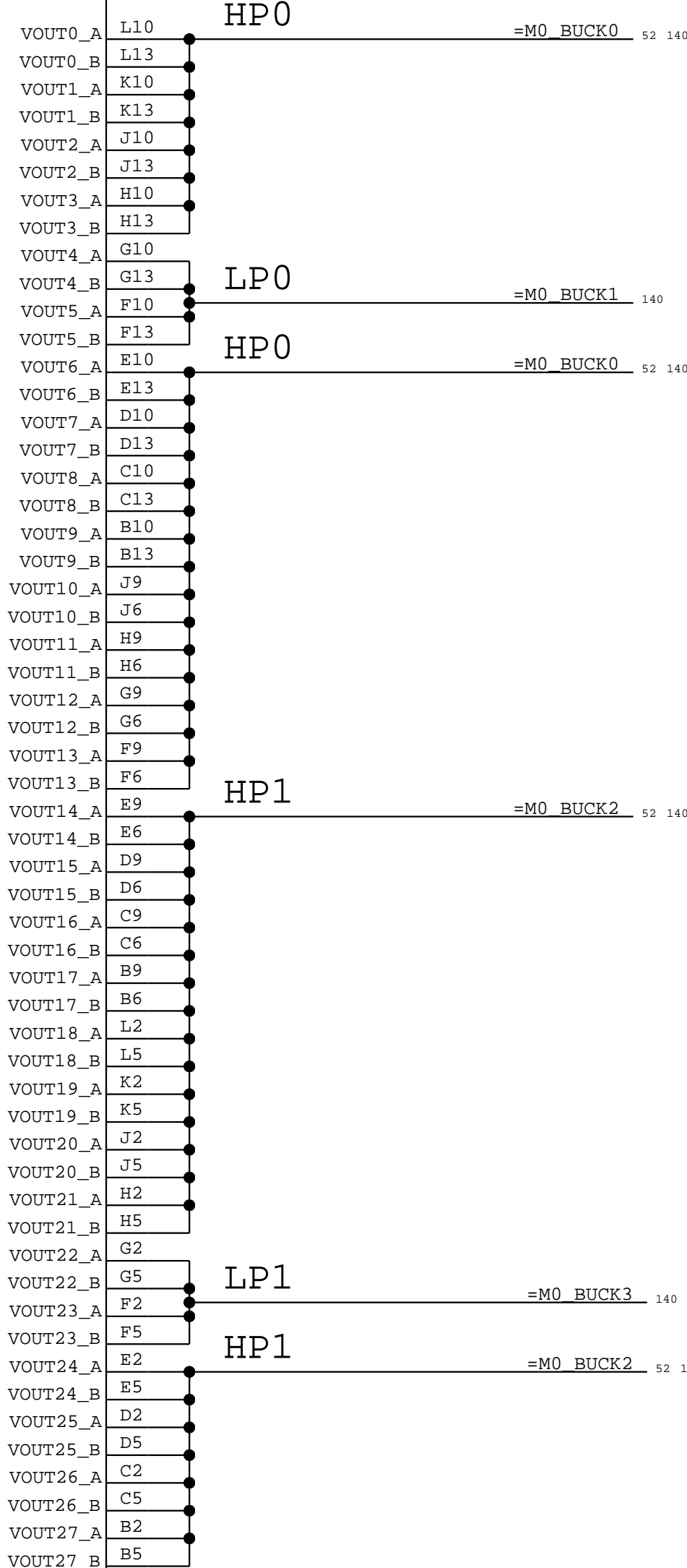
MONACO_0

INSTANCE = C0
SILICON:CFG = A0:A0, B0:D0
SILICON:OTP = A0:ZP_, B0:YP_



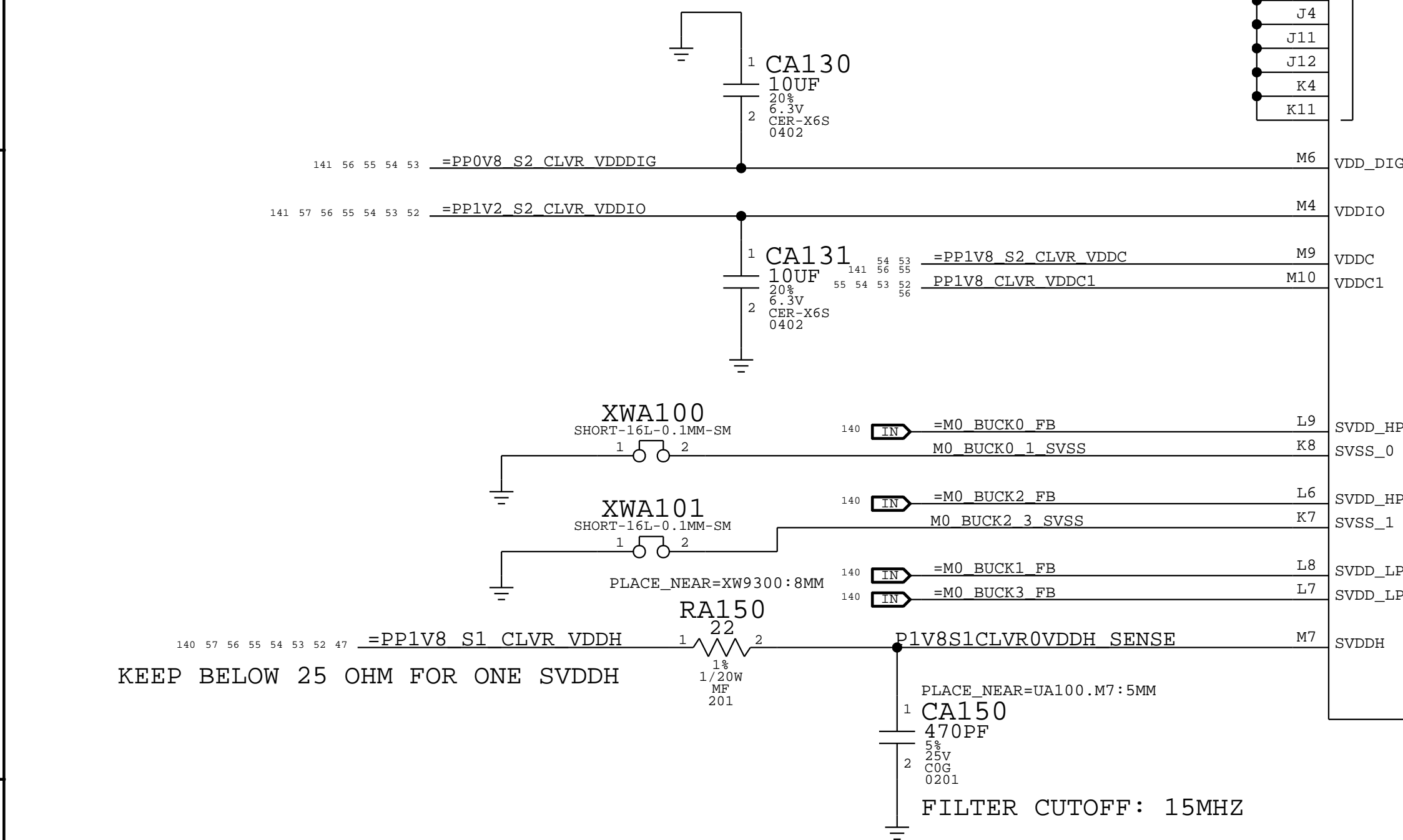
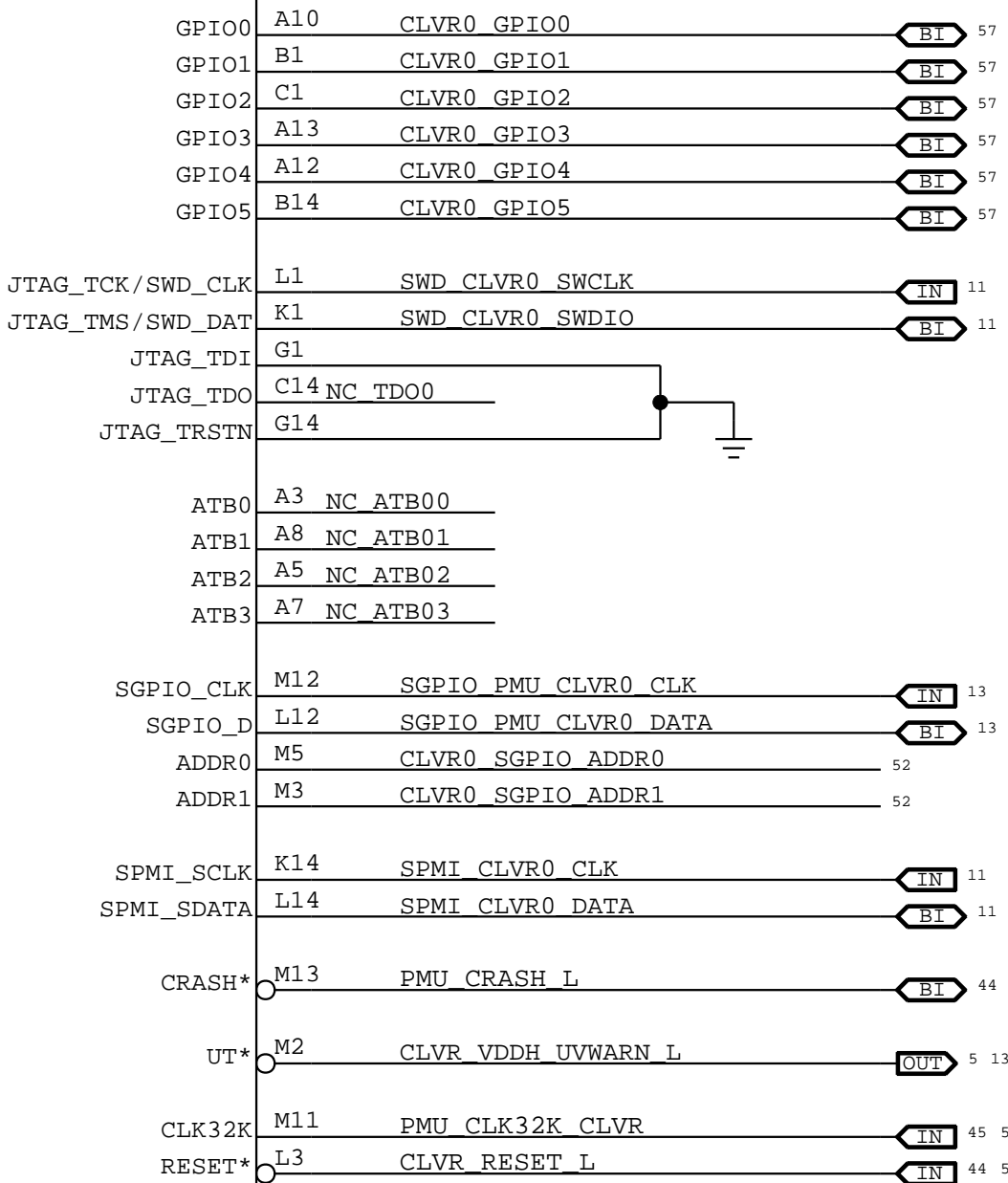
OMIT_TABLE

UA100
MON
BGA
SYM 1 OF 2

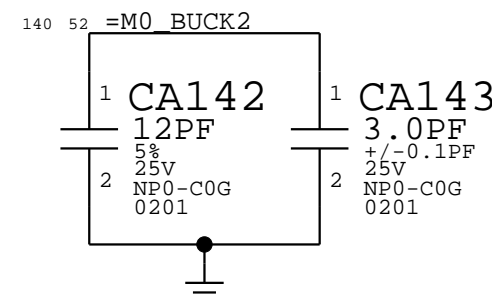
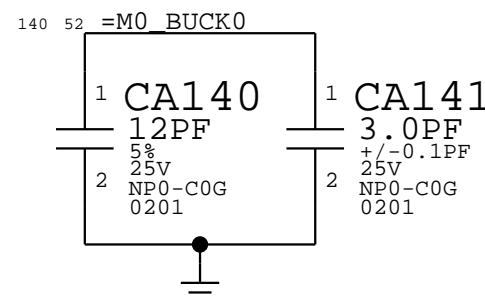


OMIT_TABLE

UA100
MON
BGA
SYM 2 OF 2



VOLTAGE=1.8V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
PP1V8_CLVR_VDDC1
MAKE_BASE=TRUE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-23128	1	IC,MCM,B0,OTP-YPF,DEV,FCCSP168_REV8	UA100	CRITICAL	

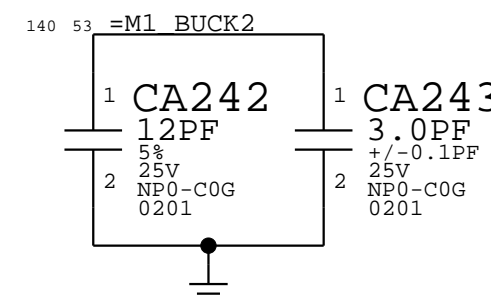
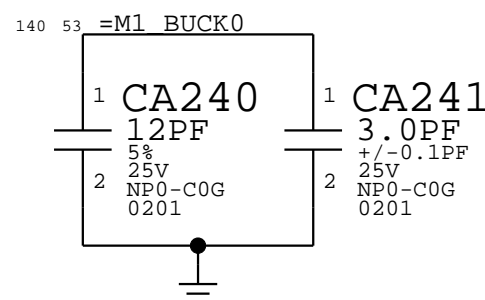
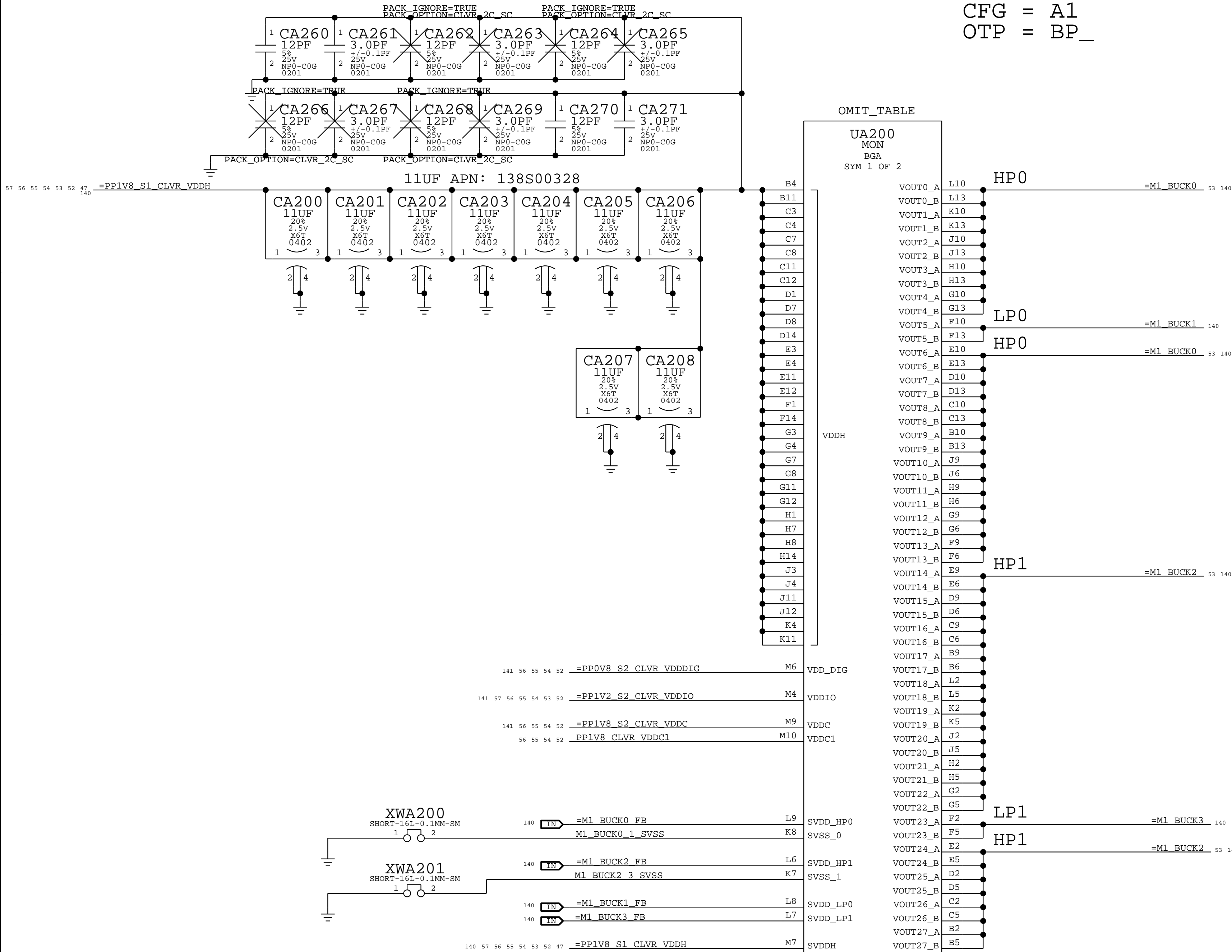
BOM_COST_GROUP=SOC POWER

PAGE TITLE			
MONACO 0			
	DRAWING NUMBER	051-06558	SIZE D
	REVISION	2.0.0	
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OK2INTEGRATE

MONACO_1

INSTANCE = C1
CFG = A1
OTP = BP_



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-23123	1	IC,MON,B0,OTP-BPF,DEV,FCCSP168,REV8	UA200	CRITICAL	

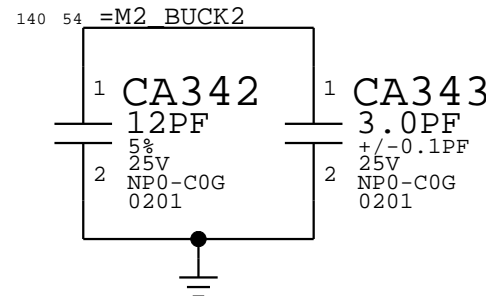
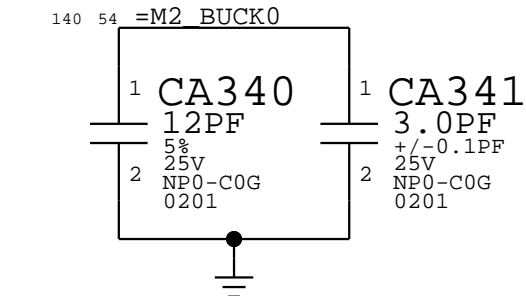
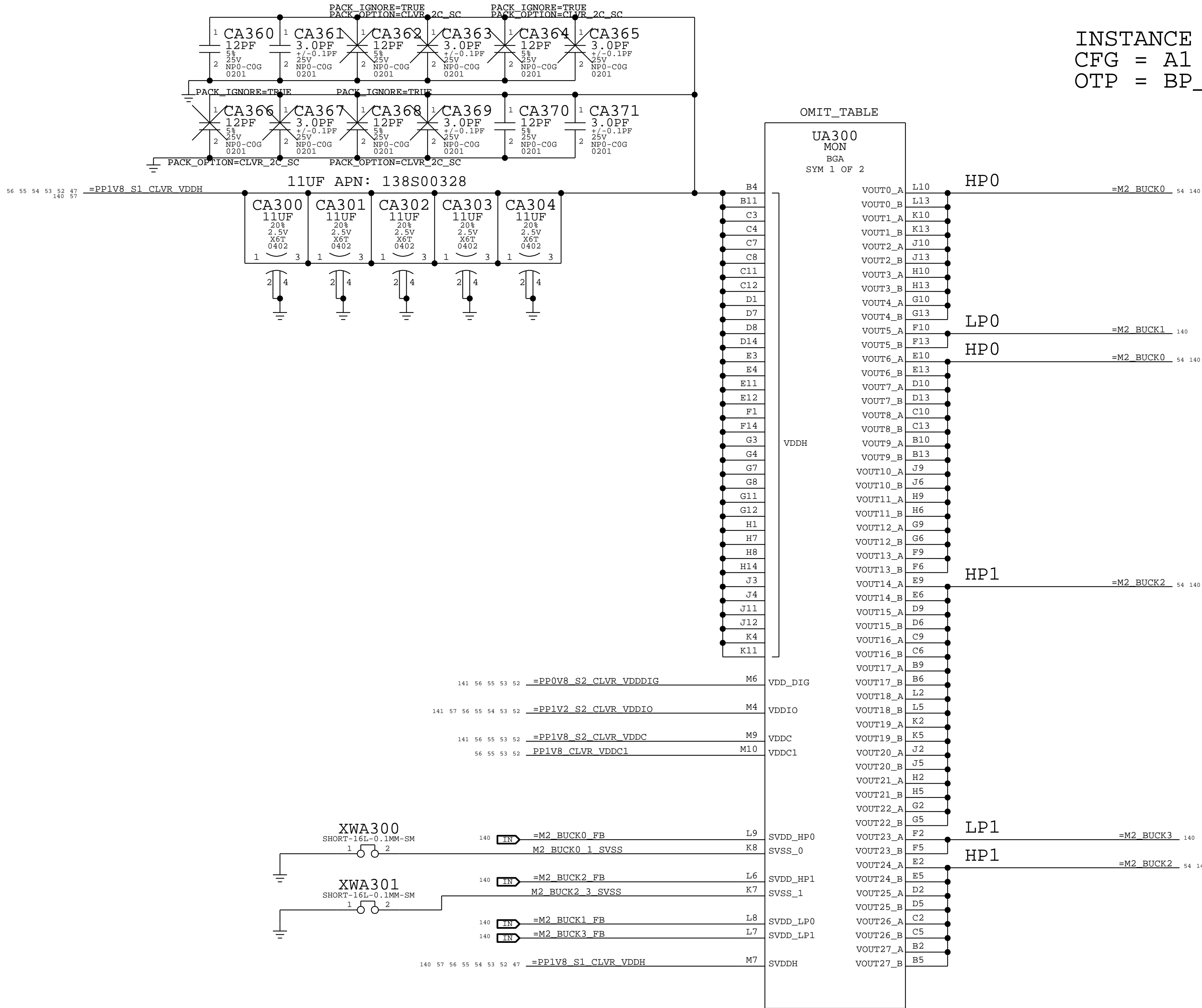
BOM_COST_GROUP=SOC POWER

PAGE TITLE			
MONACO 1			
	DRAWING NUMBER	051-06558	SIZE D
	REVISION	2.0.0	
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OK2INTEGRATE


MONACO_2

INSTANCE = C2
CFG = A1
OTP = BP_

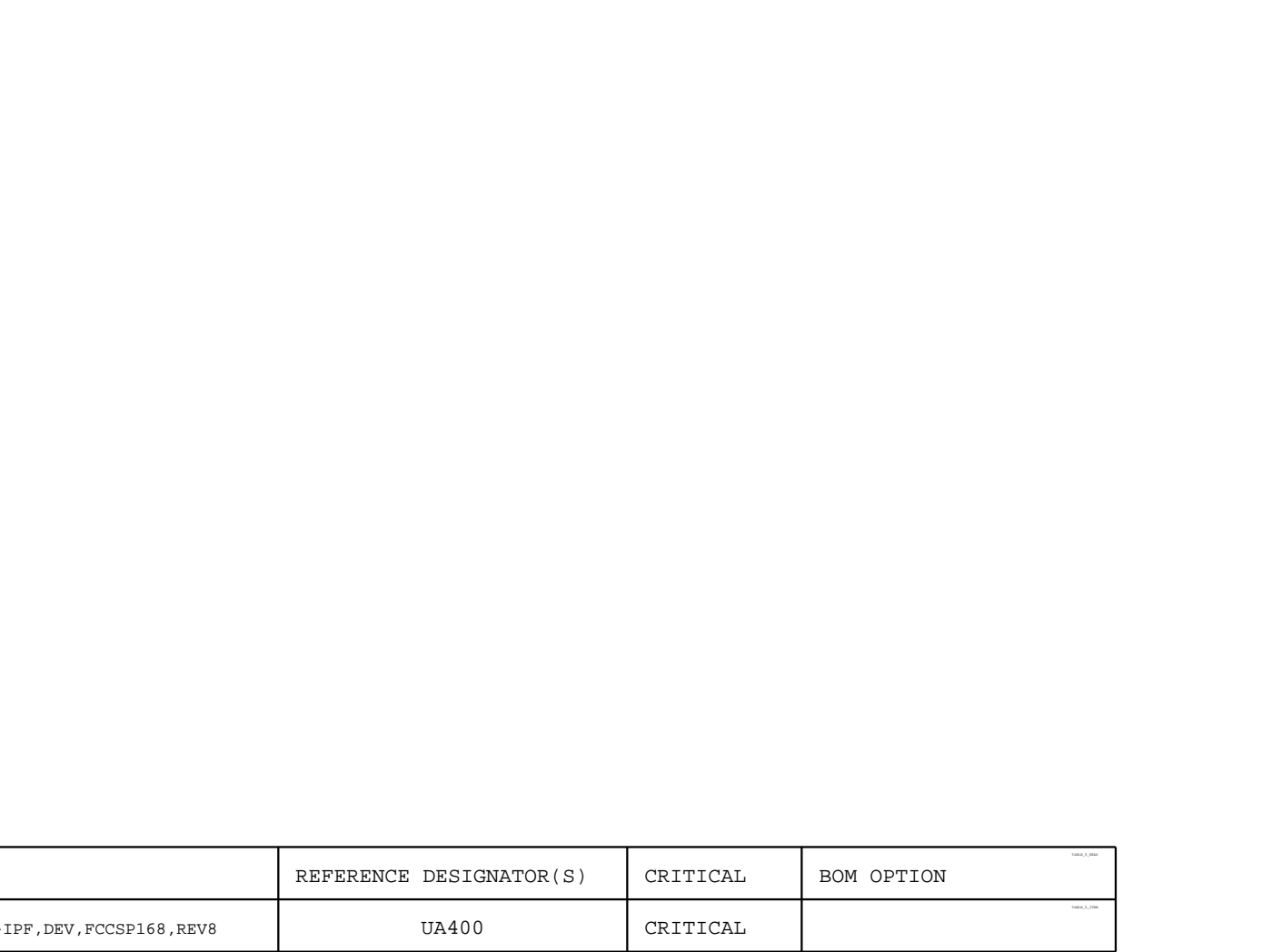
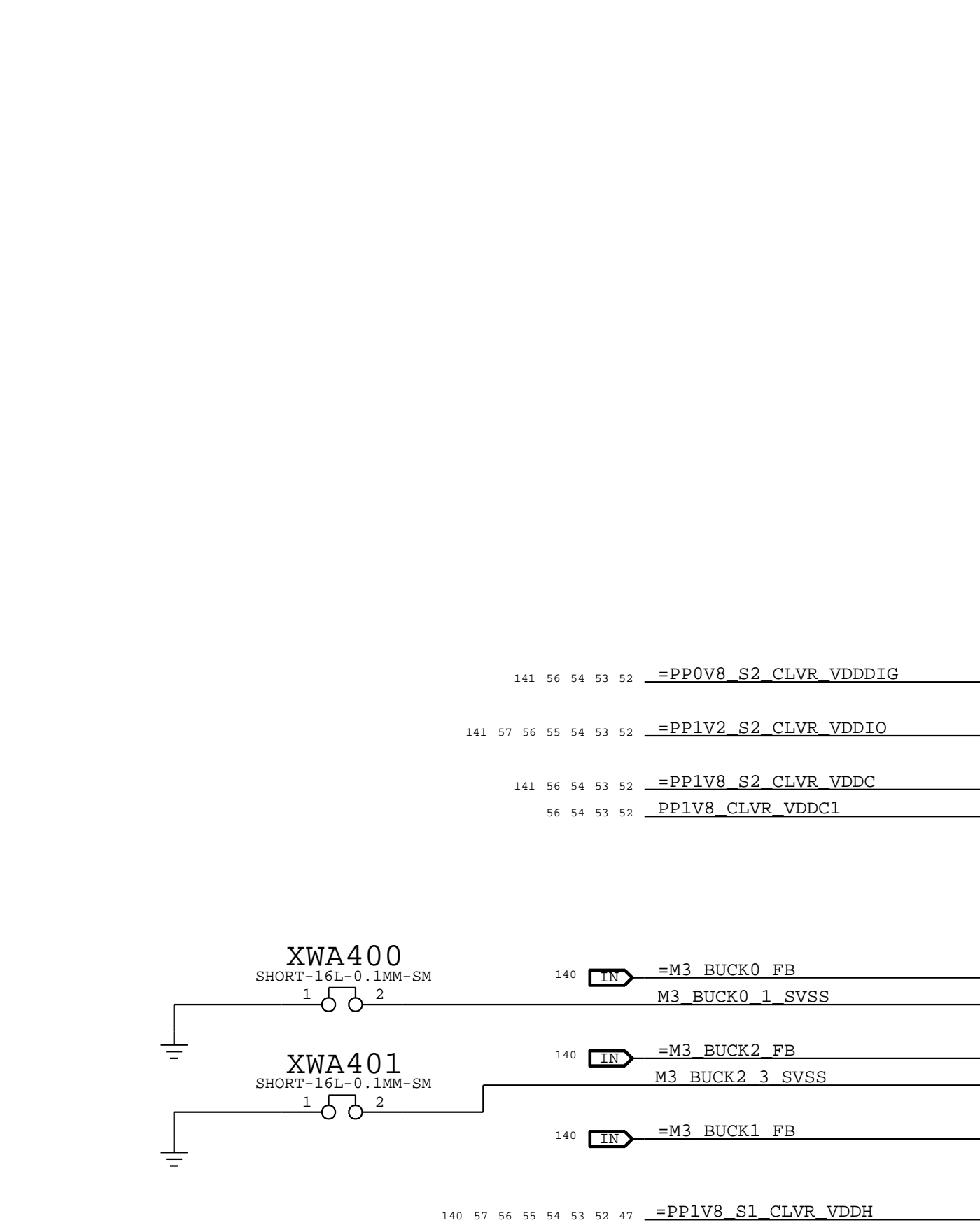
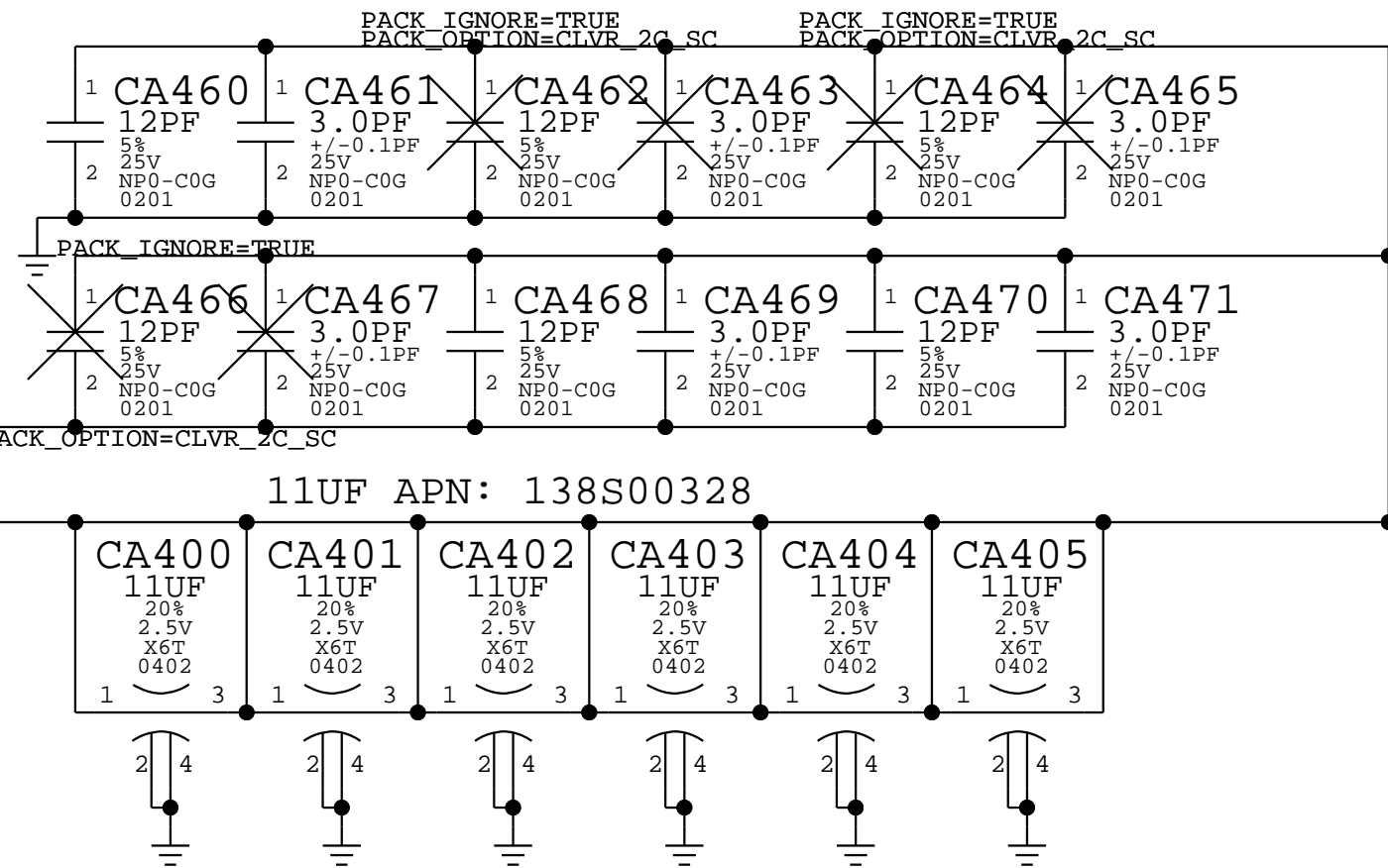


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-23123	1	IC,MON,B0,OTP-BFP,DEV,FOCSP168,REV8	UA300	CRITICAL	

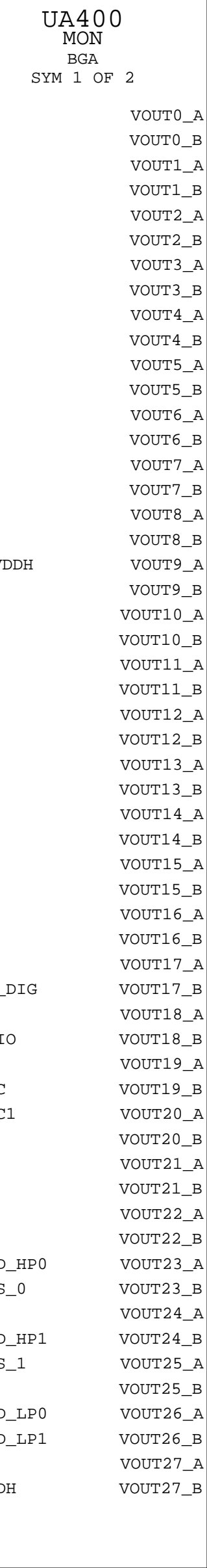
BOM_COST_GROUP=SOC POWER

PAGE TITLE			
MONACO 2			
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OK2INTEGRATE



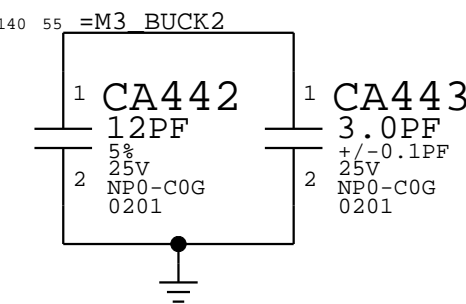
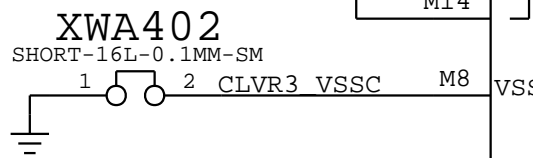
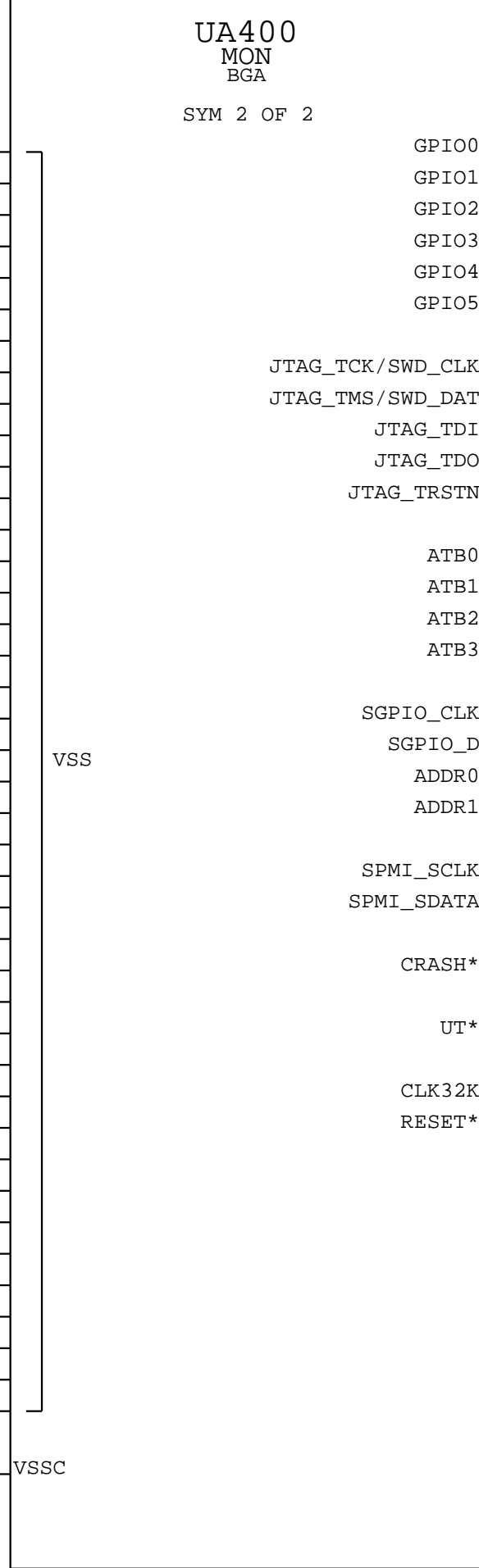
OMIT_TABLE



INSTANCE = C3
CFG = B0
OTP = IP_

MONACO_3

OMIT_TABLE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-23124	1	IC,MON,B0,OTP-IPF,DEV,FCOSP168,REV8	UA400	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE		
MONACO 3		
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OK2INTEGRATE

MONACO_4

SC

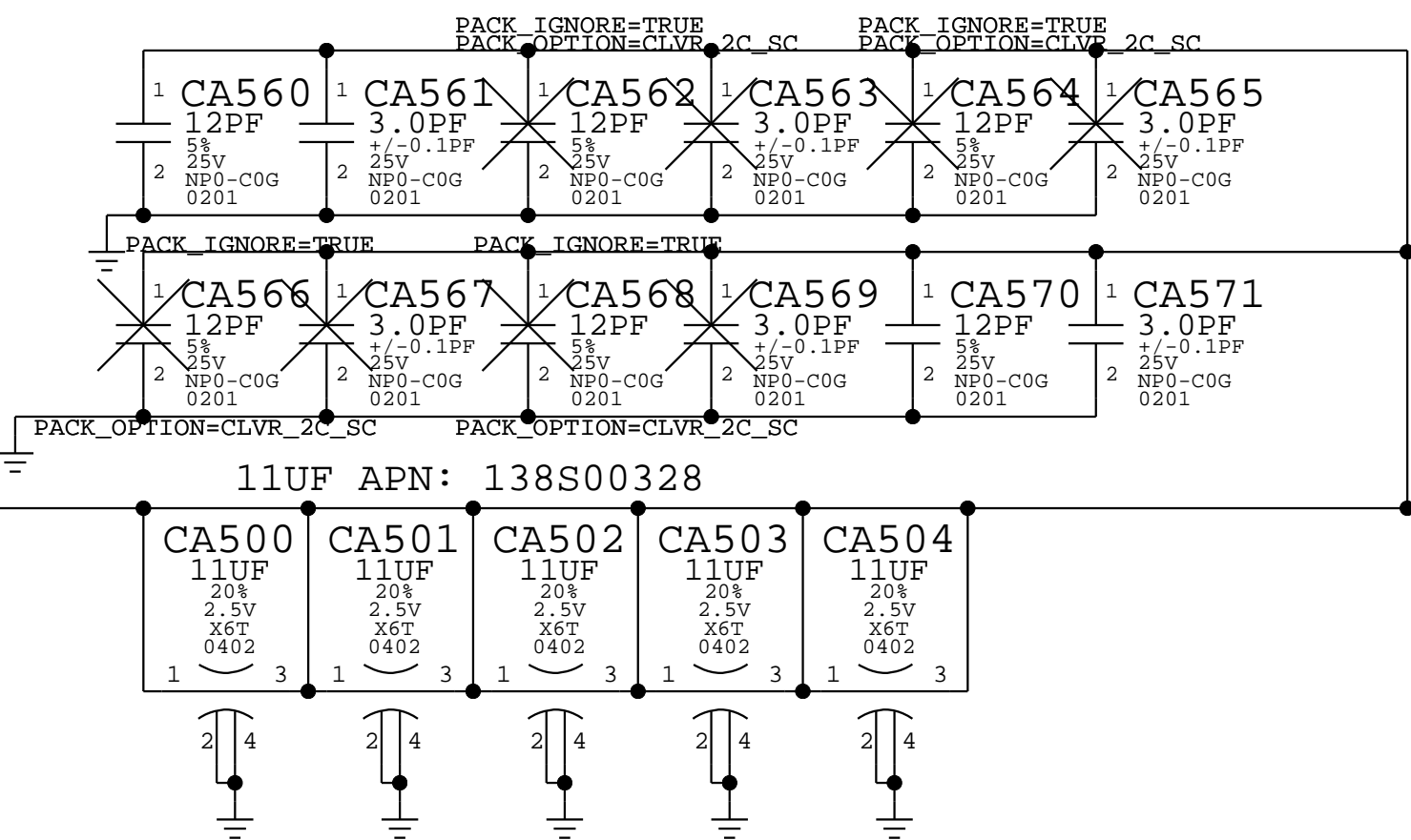
1C

2C

INSTANCE = C2
CFG = C0
OTP = QP_

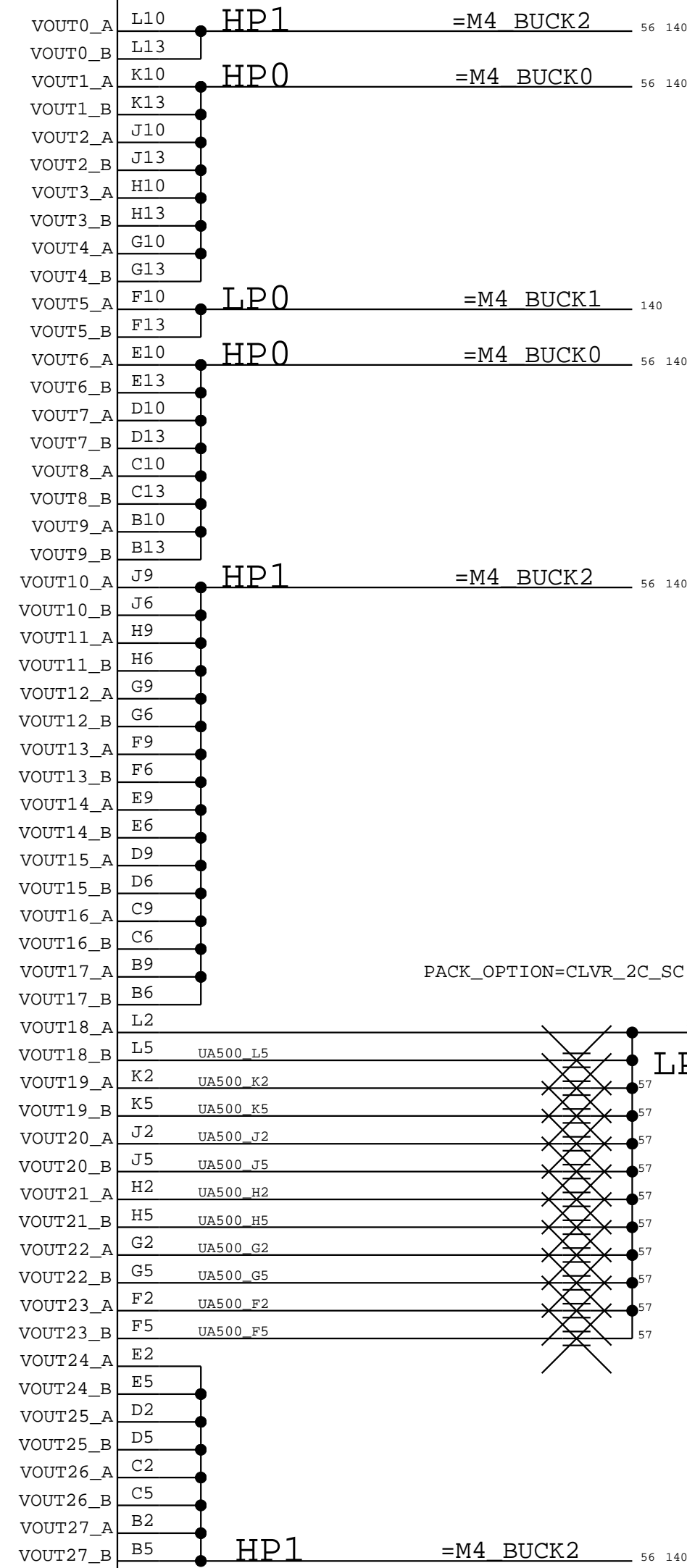
INSTANCE = C4
CFG = C1
OTP = RP_

INSTANCE = C4
CFG = C2
OTP = SP_



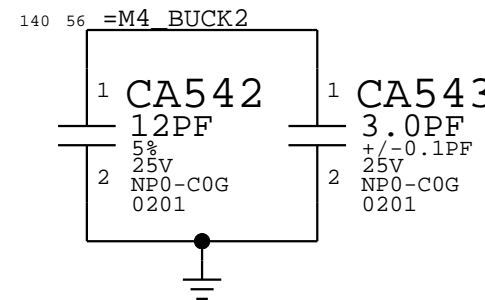
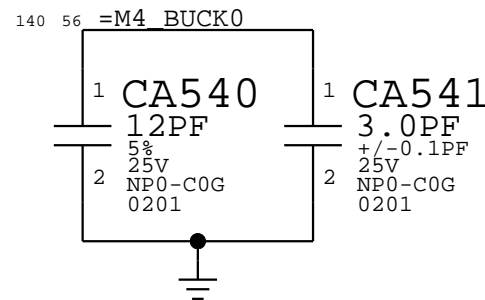
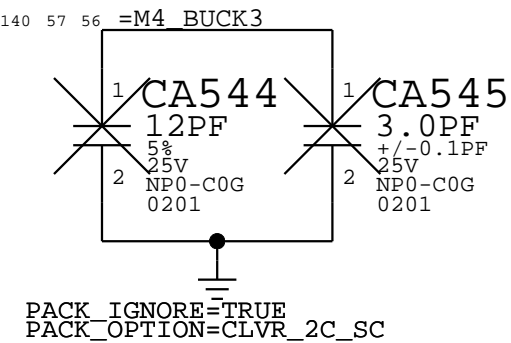
OMIT_TABLE

UA500
MON
BGA
SYM 1 OF 2




OMIT_TABLE

UA500
MON
BGA
SYM 2 OF 2



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-23125	1	1C,MON,B0,OTP-QPF,DEV,FCCSP168.REV8	UA500	CRITICAL	MONACO_SC
998-23126	1	1C,MON,B0,OTP-RPF,DEV,FCCSP168.REV8	UA500	CRITICAL	MONACO_1C

BOM_COST_GROUP=SOC POWER

PAGE TITLE			
MONACO 4			
 Apple Inc.	DRAWING NUMBER	051-06558	SIZE D
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		PAGE	105 OF 998
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D

C

B

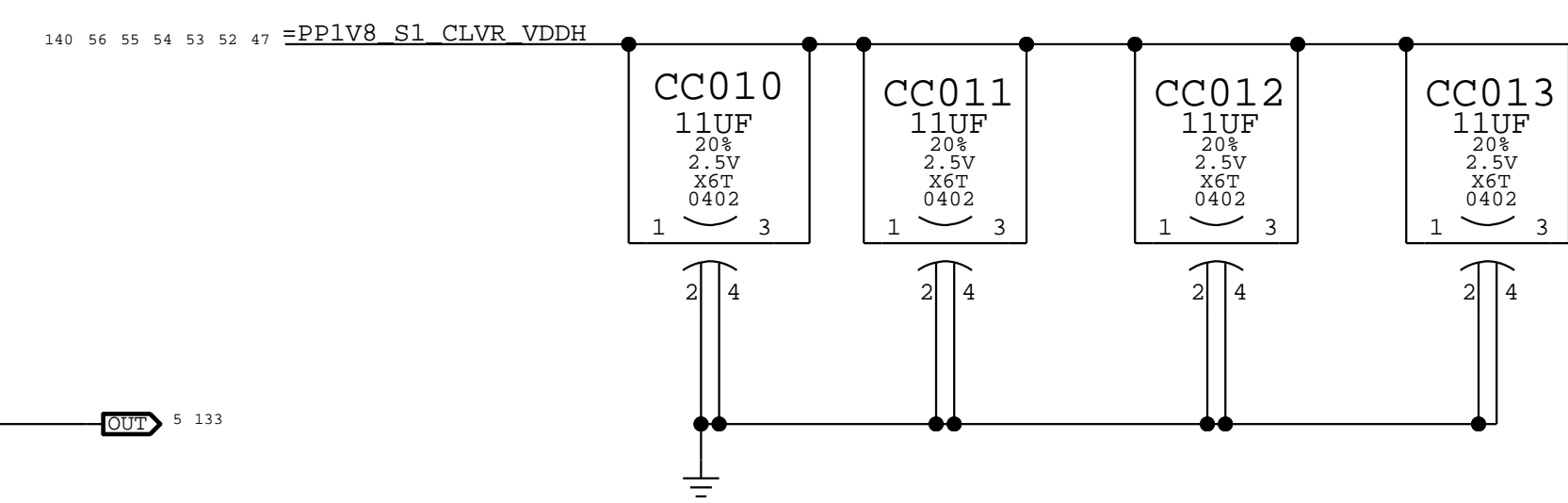
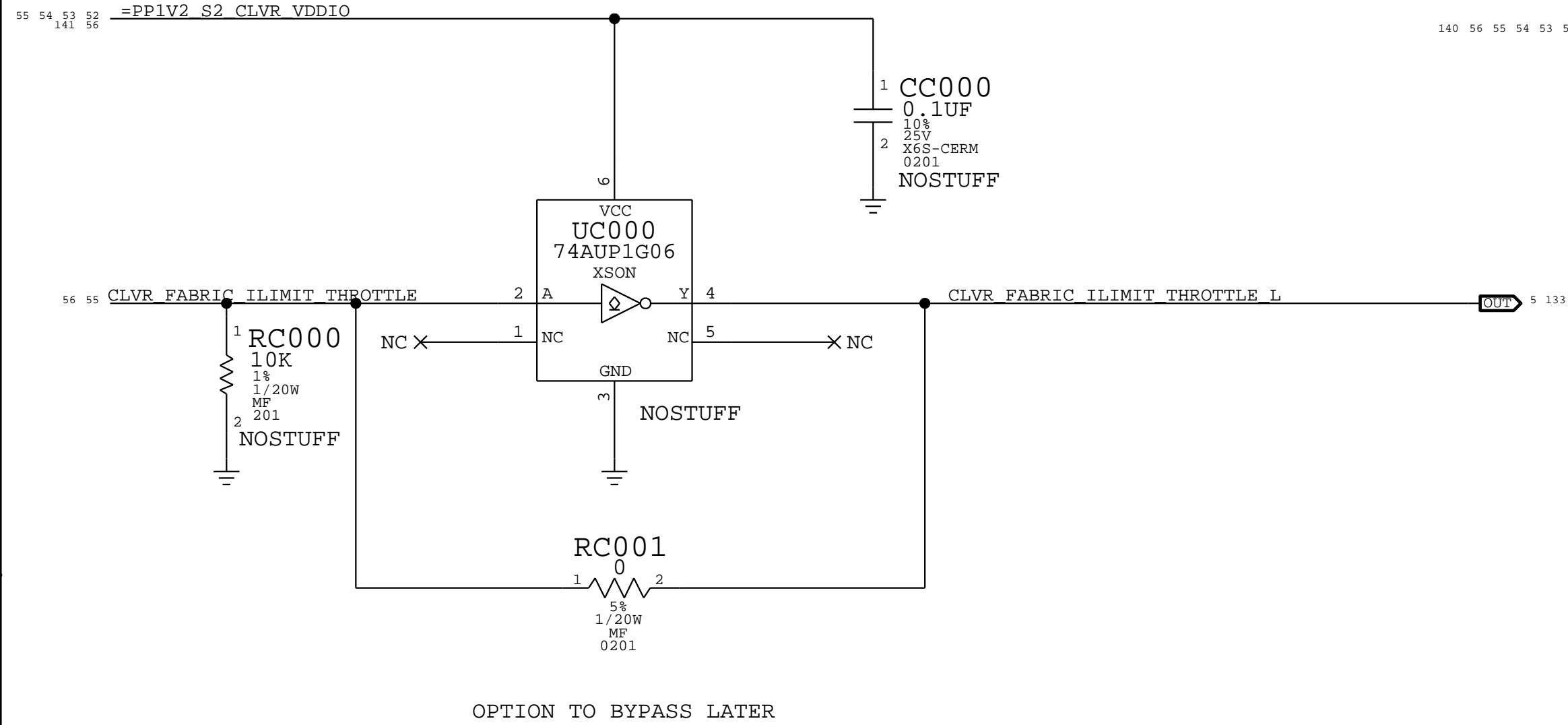
A

D

C

B

A



MONACO UNUSED GPIO's

MAKE_BASE=TRUE		
CLVR0 GPIO0	==	NC CLVR0 GPIO0
CLVR0 GPIO1	==	NC CLVR0 GPIO1
CLVR0 GPIO2	==	NC CLVR0 GPIO2
CLVR0 GPIO3	==	NC CLVR0 GPIO3
CLVR0 GPIO4	==	NC CLVR0 GPIO4
CLVR0 GPIO5	==	NC CLVR0 GPIO5
MAKE_BASE=TRUE		
CLVR1 GPIO0	==	NC CLVR1 GPIO0
CLVR1 GPIO1	==	NC CLVR1 GPIO1
CLVR1 GPIO2	==	NC CLVR1 GPIO2
CLVR1 GPIO3	==	NC CLVR1 GPIO3
CLVR1 GPIO4	==	NC CLVR1 GPIO4
CLVR1 GPIO5	==	NC CLVR1 GPIO5
MAKE_BASE=TRUE		
CLVR2 GPIO0	==	NC CLVR2 GPIO0
CLVR2 GPIO1	==	NC CLVR2 GPIO1
CLVR2 GPIO2	==	NC CLVR2 GPIO2
CLVR2 GPIO3	==	NC CLVR2 GPIO3
CLVR2 GPIO4	==	NC CLVR2 GPIO4
CLVR2 GPIO5	==	NC CLVR2 GPIO5
MAKE_BASE=TRUE		
CLVR3 GPIO0	==	NC CLVR3 GPIO0
CLVR3 GPIO1	==	NC CLVR3 GPIO1
CLVR3 GPIO3	==	NC CLVR3 GPIO3
CLVR3 GPIO4	==	NC CLVR3 GPIO4
CLVR3 GPIO5	==	NC CLVR3 GPIO5
MAKE_BASE=TRUE		
CLVR4 GPIO0	==	NC CLVR4 GPIO0
CLVR4 GPIO1	==	NC CLVR4 GPIO1
CLVR4 GPIO2	==	NC CLVR4 GPIO2
CLVR4 GPIO3	==	NC CLVR4 GPIO3
CLVR4 GPIO4	==	NC CLVR4 GPIO4
CLVR4 GPIO5	==	NC CLVR4 GPIO5

MONACO resolution between sC/lC deltas

CLVR4 BUCK3 is NC/unused in 1C, but the pins need net names to allow rel vias in pad

MAKE_BASE=TRUE		
M4 BUCK3	==	UA500 L2 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 L5 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 K2 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 K5 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 J2 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 J5 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 H2 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 H5 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 G2 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 G5 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 F2 CKPLUS_WAIVE=SINGLE_NODENET
	==	UA500 F5 CKPLUS_WAIVE=SINGLE_NODENET

BOM_COST_GROUP=PLATFORM_POWER

PAGE TITLE		
MONACO PROJECT SUPPORT		
	DRAWING NUMBER	051-06558
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* OK2INTEGRATE *

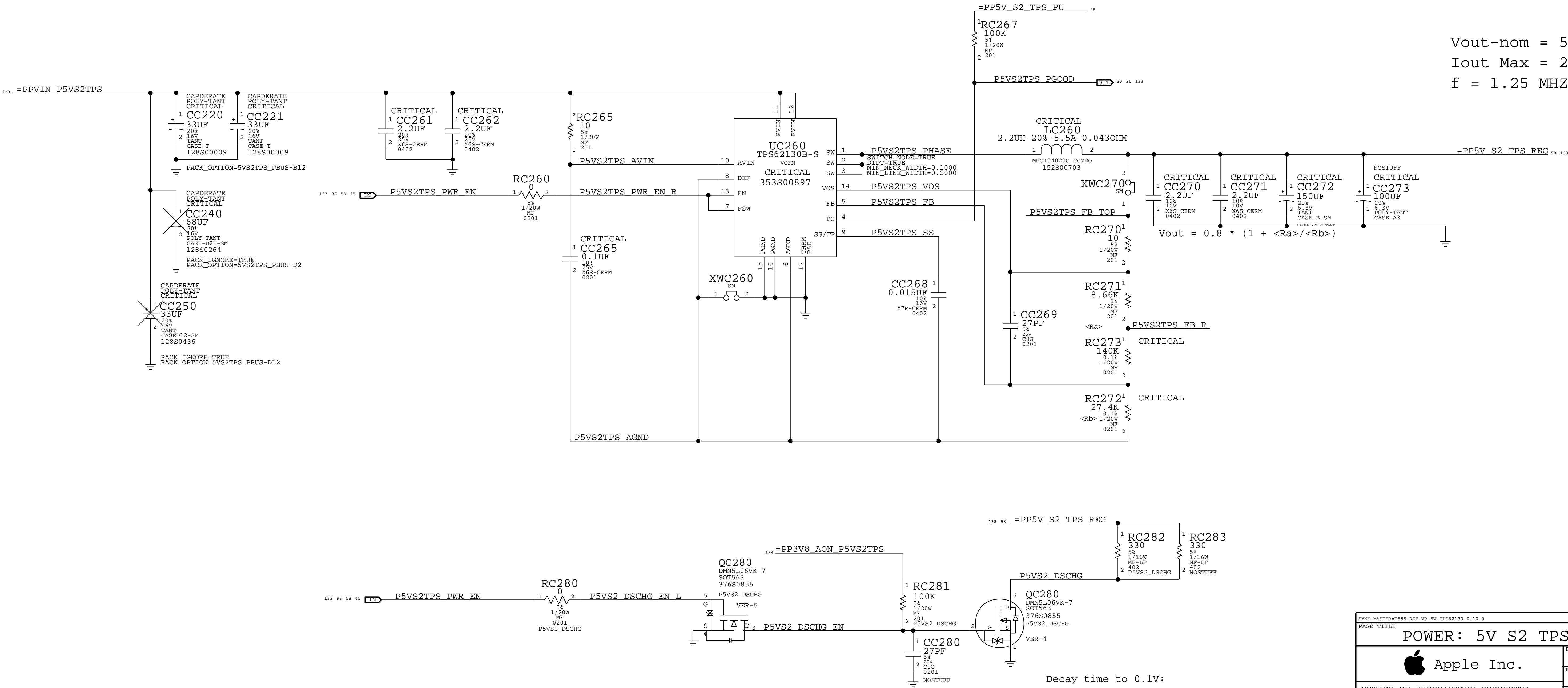
5V_S2 Voltage Regulator (low power option)

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5VS2TPS_PBUS-B12
PACK_OPTION=5VS2TPS_PBUS-D2
PACK_OPTION=5VS2TPS_PBUS-D12

START UP TIME = 4.7/7.5/10.5 MS
(min/typ/max)

Vout-nom = 5.14V
Iout Max = 2.1A
f = 1.25 MHZ



Decay time to 0.1V:
225ms-min / 327ms-typ / 420ms-max
(Vout=5.14V5%, Cout=250uF20%, R=330R5%)

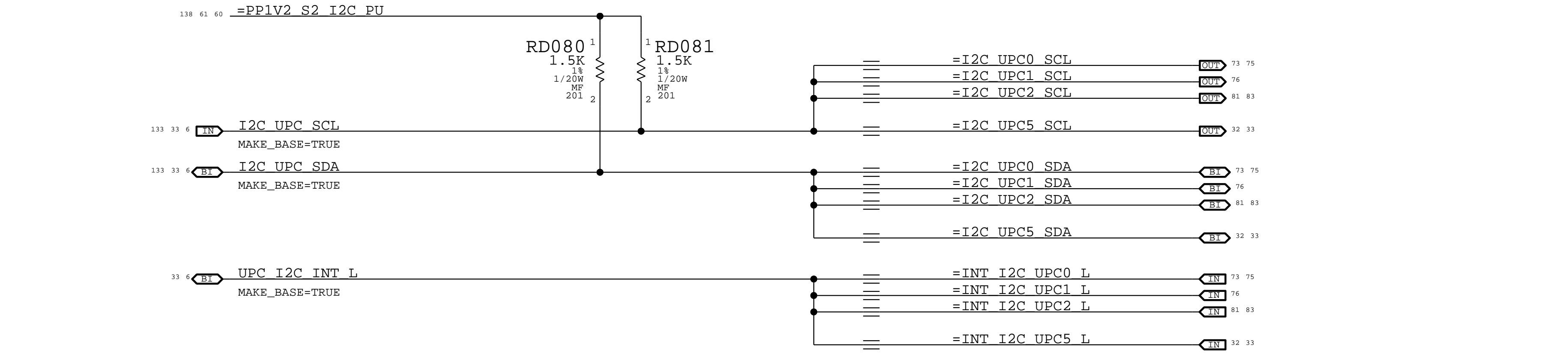
POWER: 5V S2 TPS62130		
Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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BOM_COST_GROUP=PLATFORM POWER

AP_I2C0

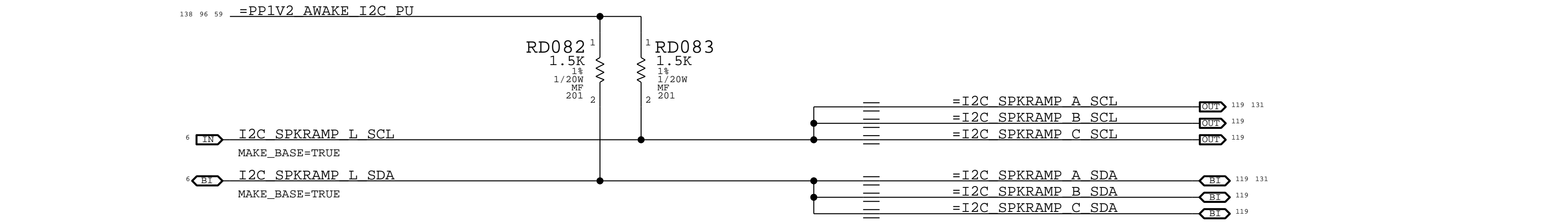
DEVICE	CARD/REFDES	7-BIT	8-BIT
ACE2 - 0 (DEBUG)	USB-C 0	0X38	0X70
ACE2 - 1 (DEBUG)	USB-C 0	0X3F	0X7E
ACE2 - 2 (DEBUG)	USB-C 1	0X3B	0X76
ACE2 - 5 (DEBUG)	USB-C 1	0X3A	0X74
BANK ALL CALL		0X6B	0XD6

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
?	?	?	?	?	?
?	?	?	?	?	?
?	?	?	?	?	?



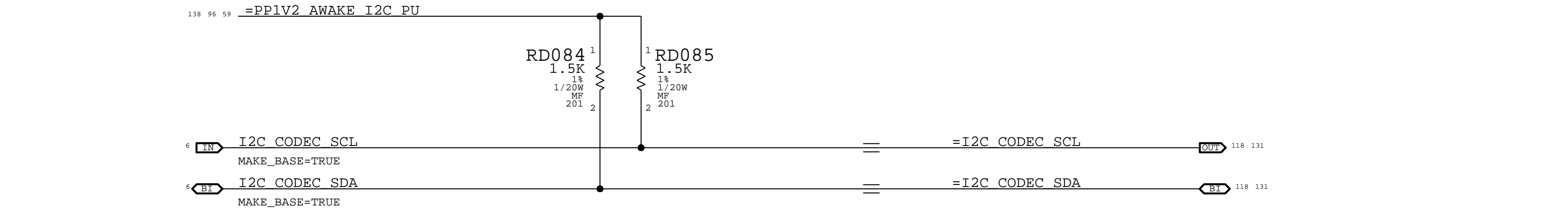
AP_I2C1

DEVICE	CARD/REFDES	7-BIT	8-BIT
SPKRAMP TAWANG A	SPKRAMP	0X38	0X70
SPKRAMP TAWANG B	SPKRAMP	0X39	0X72
SPKRAMP TAWANG C	SPKRAMP	0X3A	0X74



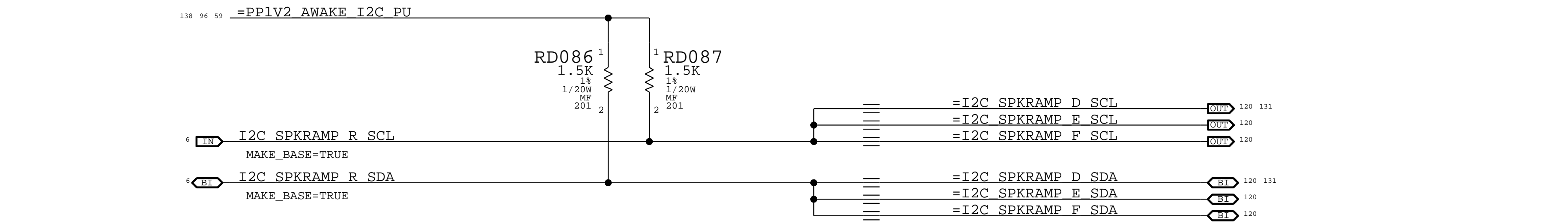
AP_I2C2

DEVICE	CARD/REFDES	7-BIT	8-BIT
CODEC - CLIFDEN	DMIC & CODEC	0X48	0X90
CODEC - CARLOW	DMIC & CODEC	0X4B	0X95



AP_I2C3

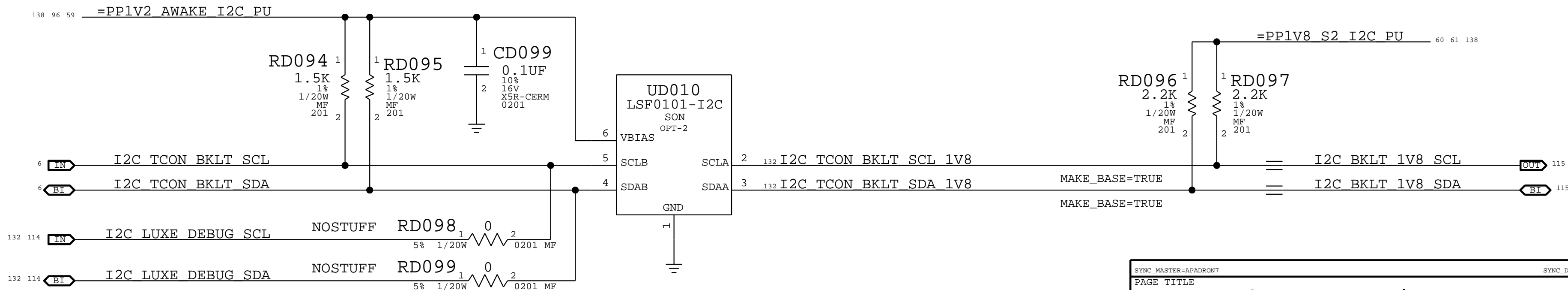
DEVICE	CARD/REFDES	7-BIT	8-BIT
SPKRAMP TAWANG D	SPKRAMP	0X3B	0X76
SPKRAMP TAWANG E	SPKRAMP	0X3C	0X78
SPKRAMP TAWANG F	SPKRAMP	0X3D	0X7A



AP_I2C7

DEVICE	CARD/REFDES	7-BIT	8-BIT
Avellino PMIC	Display	0XXX	0XX

I2C is hooked up to testpoints on BCON brd



UNUSED:

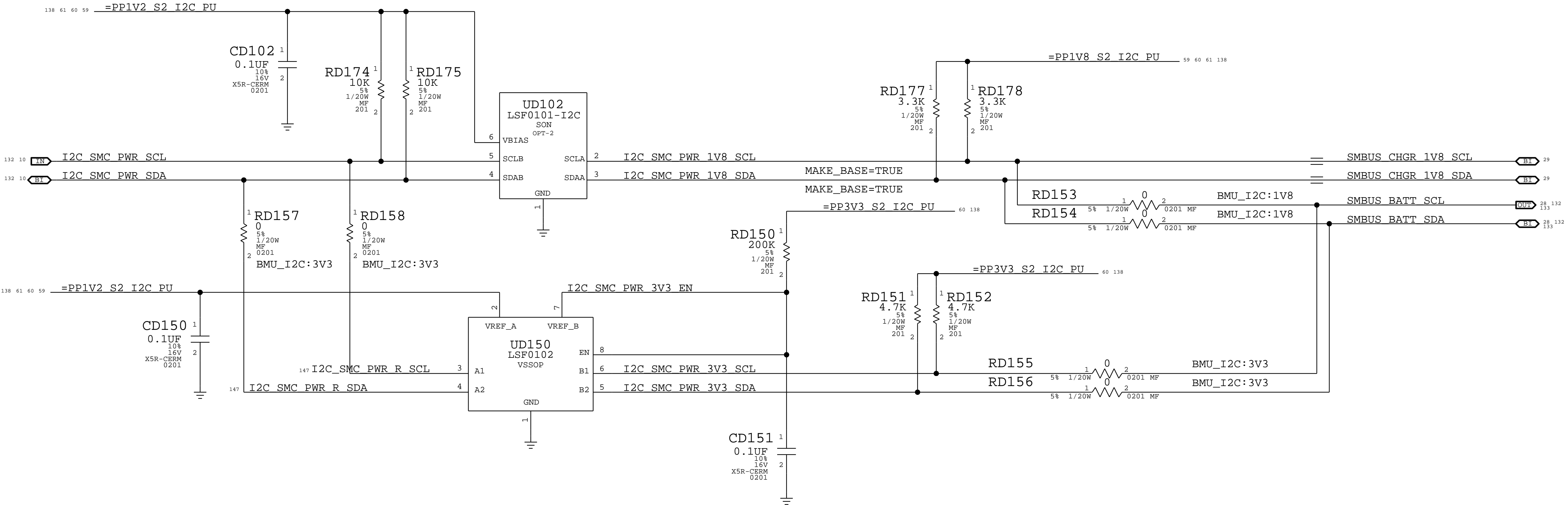
AOP_I2C1
ISP_I2C0
ISP_I2C1
ISP_I2C3

BOM_COST_GROUP=SOC

PAGE TITLE		DRAWING NUMBER		SIZE	
I2C Connections - AP		051-06558		D	
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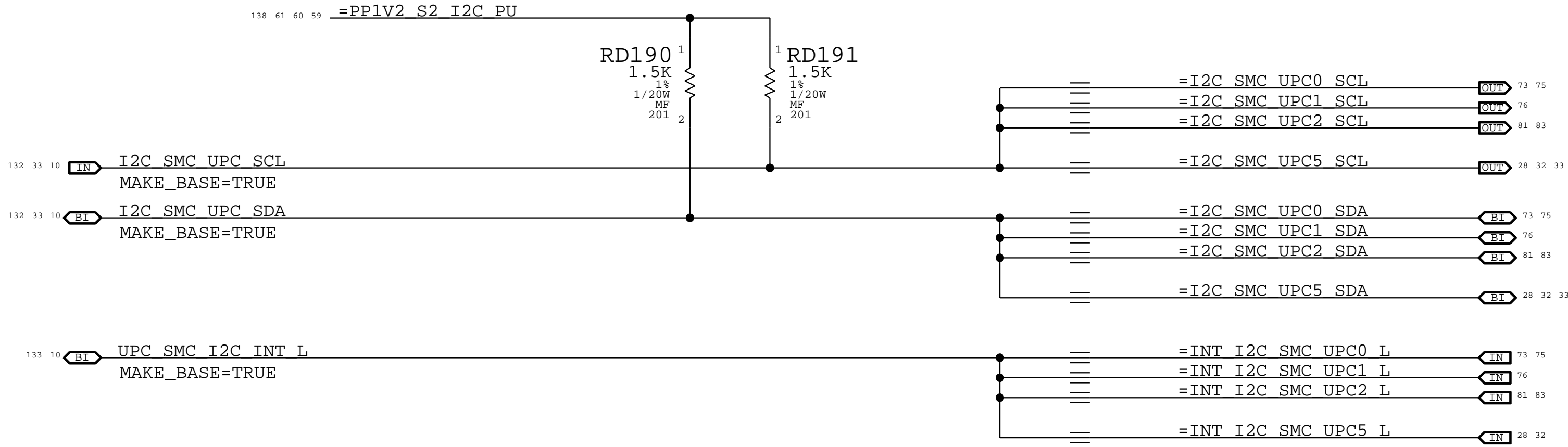
SMC_I2C0

DEVICE	CARD/REFDES	7-BIT	8-BIT
CHARGER - SUONA	BATT/CHARGER	0X09	0X12
CHARGER - WHAMOLA	BATT/CHARGER	0X??	??
ICEMAN	U5700	0XXX	0XX
BMU	BMU	0X0B	0X16



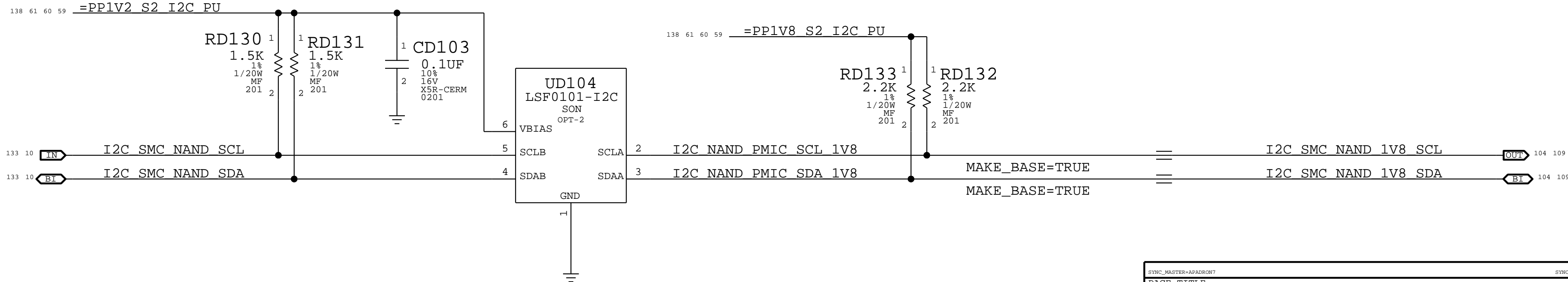
SMC_I2C1

DEVICE	CARD/REFDES	7-BIT	8-BIT
ACE2 - 0 (DEBUG)	USB-C 0	0X38	0X70
ACE2 - 1 (DEBUG)	USB-C 0	0X3F	0X7E
ACE2 - 2 (DEBUG)	USB-C 1	0X3B	0X76
ACE2 - 5 (DEBUG)	USB-C 1	0X3A	0X74
BANK1 ALL CALL		0X6B	0XD6



SMC_I2C2

DEVICE	CARD/REFDES	7-BIT	8-BIT
NAND PMIC 0	NAND 0	0X79	0XF2
NAND PMIC 1	NAND 1	0X78	0XF0




SYMC PARTS-A&ANALOGYT

SYMC_DATE=10/22/2020

PAGE TITLE

I2C Connections - SMC

 Apple Inc.

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051-06558

REVISION

2.0.0

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PAGE

131 OF 998

SHEET

60 OF 156

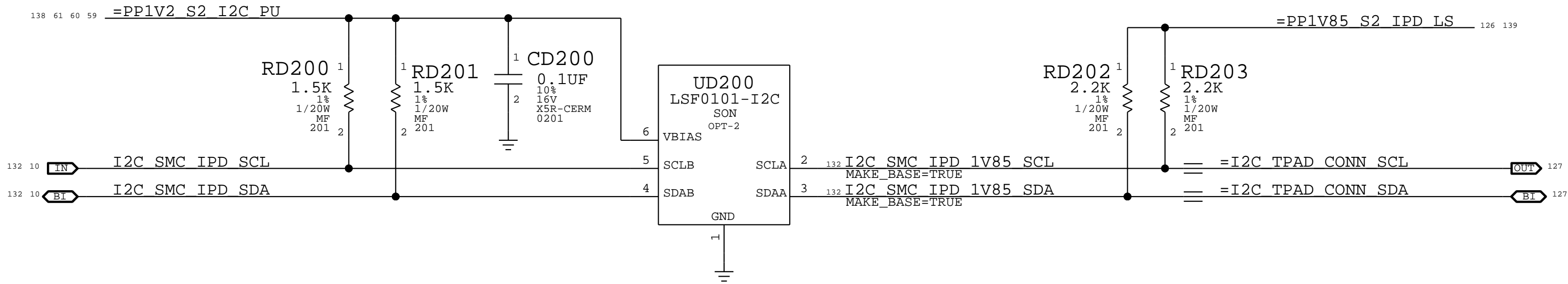
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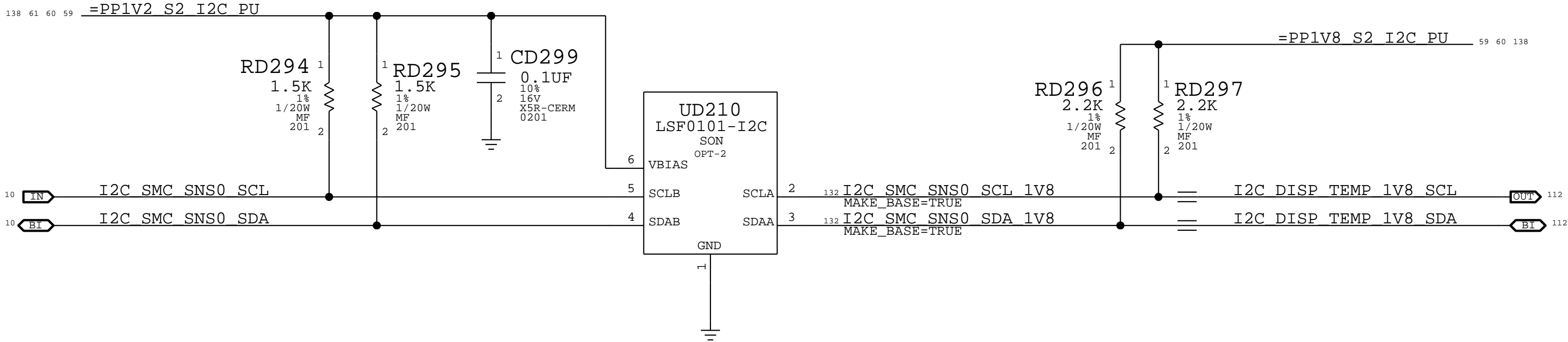
SMC_I2C3

DEVICE	CARD/REFDES	7-BIT	8-BIT
Palm Rest Temp	IPD	0X4C	0X98



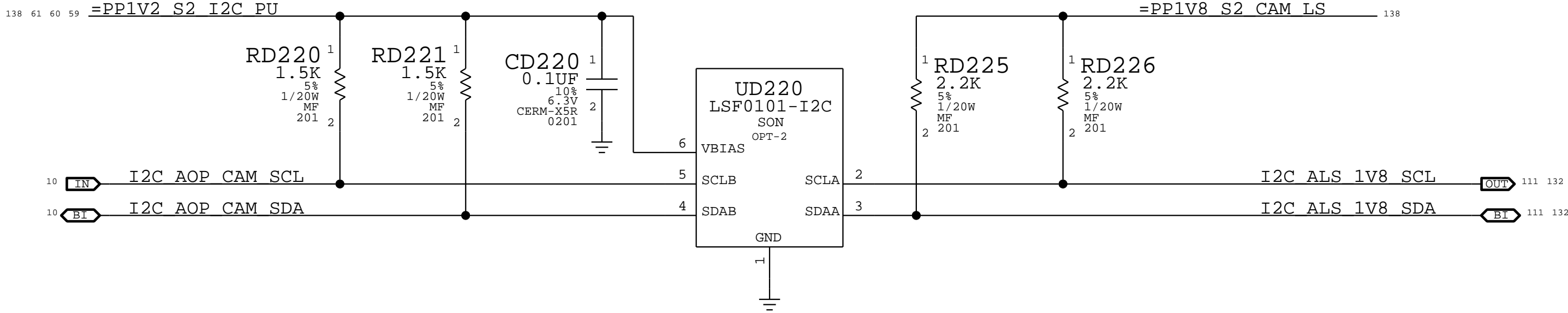
SMC_I2C4

DEVICE	CARD/REFDES	7-BIT	8-BIT
Temp Sensors	DISPLAY TEMP SNS	0X48	0X90



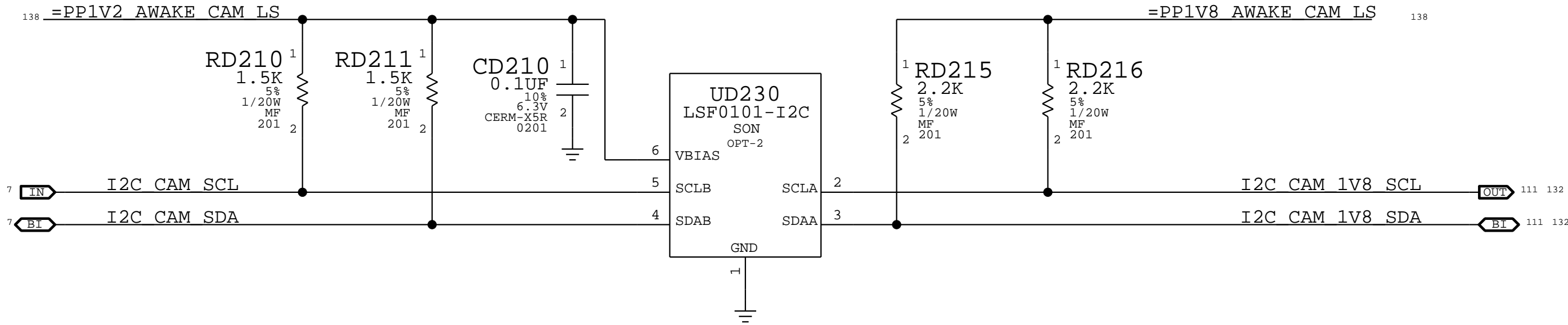
AOP_I2C0

DEVICE	CARD/REFDES	7-BIT	8-BIT
ALS	Camera	0X29	0X52
ALS Temp	Camera	0X24	0X48



ISP_I2C2

DEVICE	CARD/REFDES	7-BIT	8-BIT
FHSi+	Camera	0X10	0X20
Camera Sensor	Camera	0X6C	0XD8



UNUSED and already aliased
ISP_I2C0 SMC_I2C6
ISP_I2C1
ISP_I2C3
AOP_I2C1

SI2C

DEVICE	CARD/REFDES	7-BIT	8-BIT
SEP EEPROM	U0500	0XXX	0XX

Need to confirm if this needs/has pull-ups

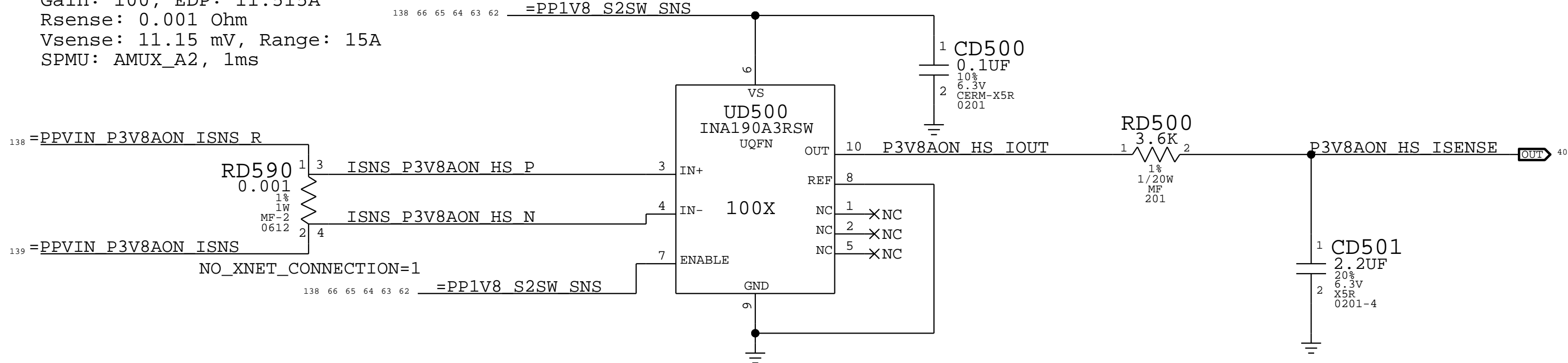
MISSING WLAN/BT, R1, CELL - VENDOR CARDS

PAGE TITLE		DRAWING NUMBER		SIZE
I2C Connections - Other		051-06558	D	
Apple Inc.		REVISION		2.0.0
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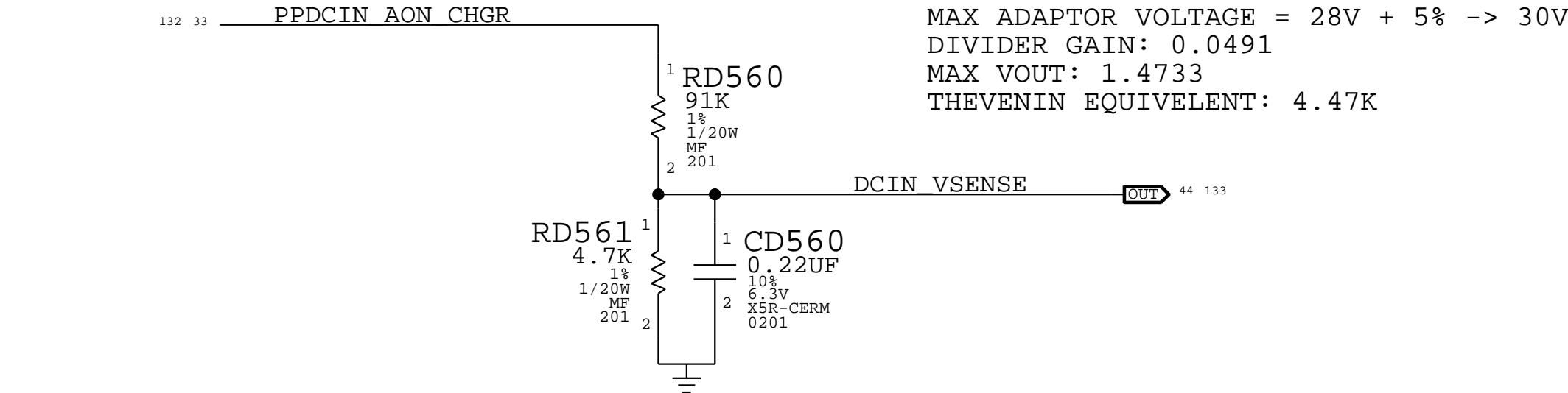
P3V8 AON HIGH SIDE ISENSE

Gain: 100, EDP: 11.515A
Rsense: 0.001 Ohm
Vsense: 11.15 mV, Range: 15A
SPMU: AMUX_A2, 1ms



DCIN VOLTAGE SENSE

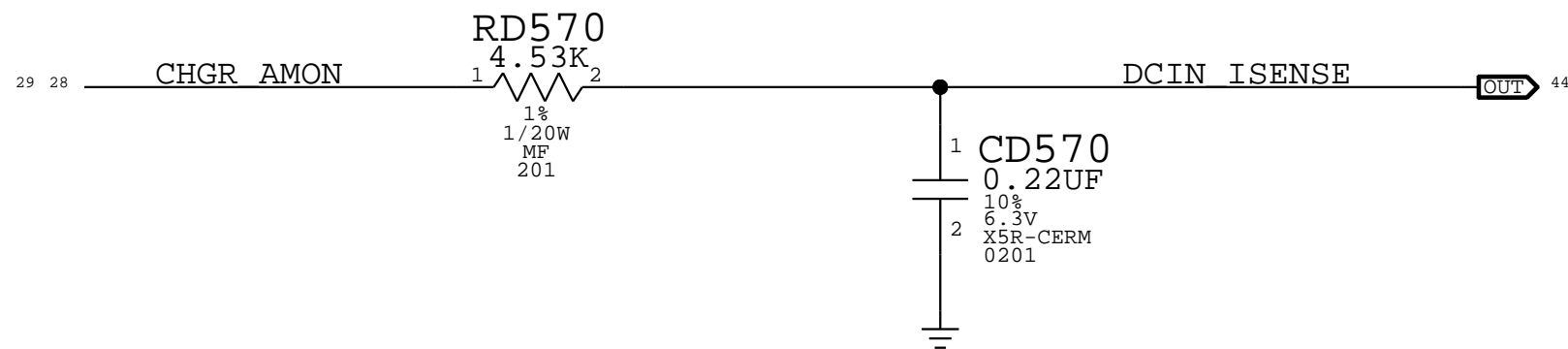
MPMU: AMUX_A0, 1ms



MAX ADAPTOR VOLTAGE = 28V + 5% -> 30V
DIVIDER GAIN: 0.0491
MAX VOUT: 1.4733
THEVENIN EQUIVELENT: 4.47K

DCIN ISENSE AMON

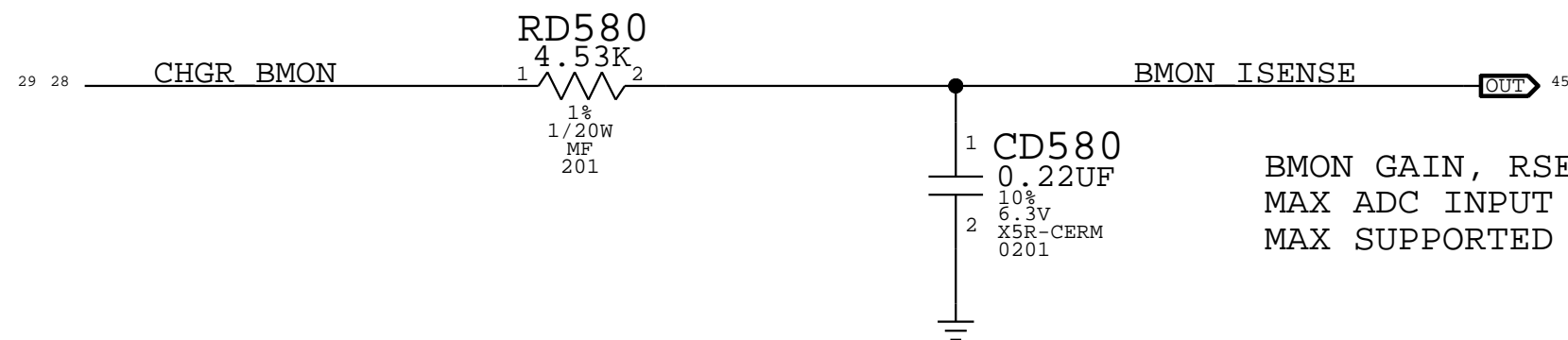
MPMU: AMUX_A1, 1ms



MAX ADAPTOR CURRENT: 5A
AMON GAIN, RSENSE: 20X, 10m
MAX AMON OUTPUT VOLTAGE: 1V

BATTERY ISENSE BMON

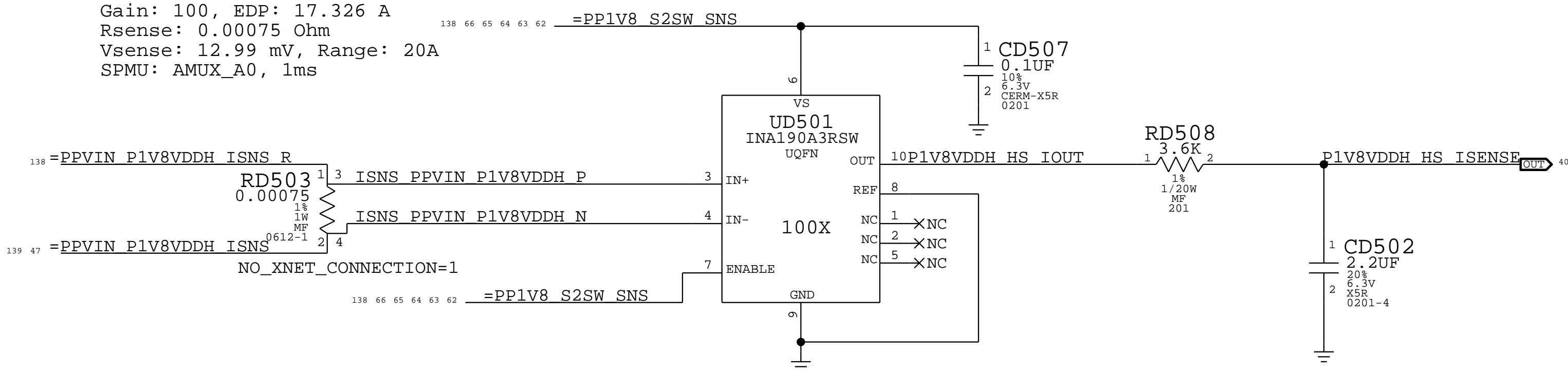
MPMU: AMUX_A2, 1ms



BMON GAIN, RSENSE: 7.9X, 5m
MAX ADC INPUT VOLTAGE: 1.5V (G=1)
MAX SUPPORTED BATTERY CURRENT SENSE: 37.97A

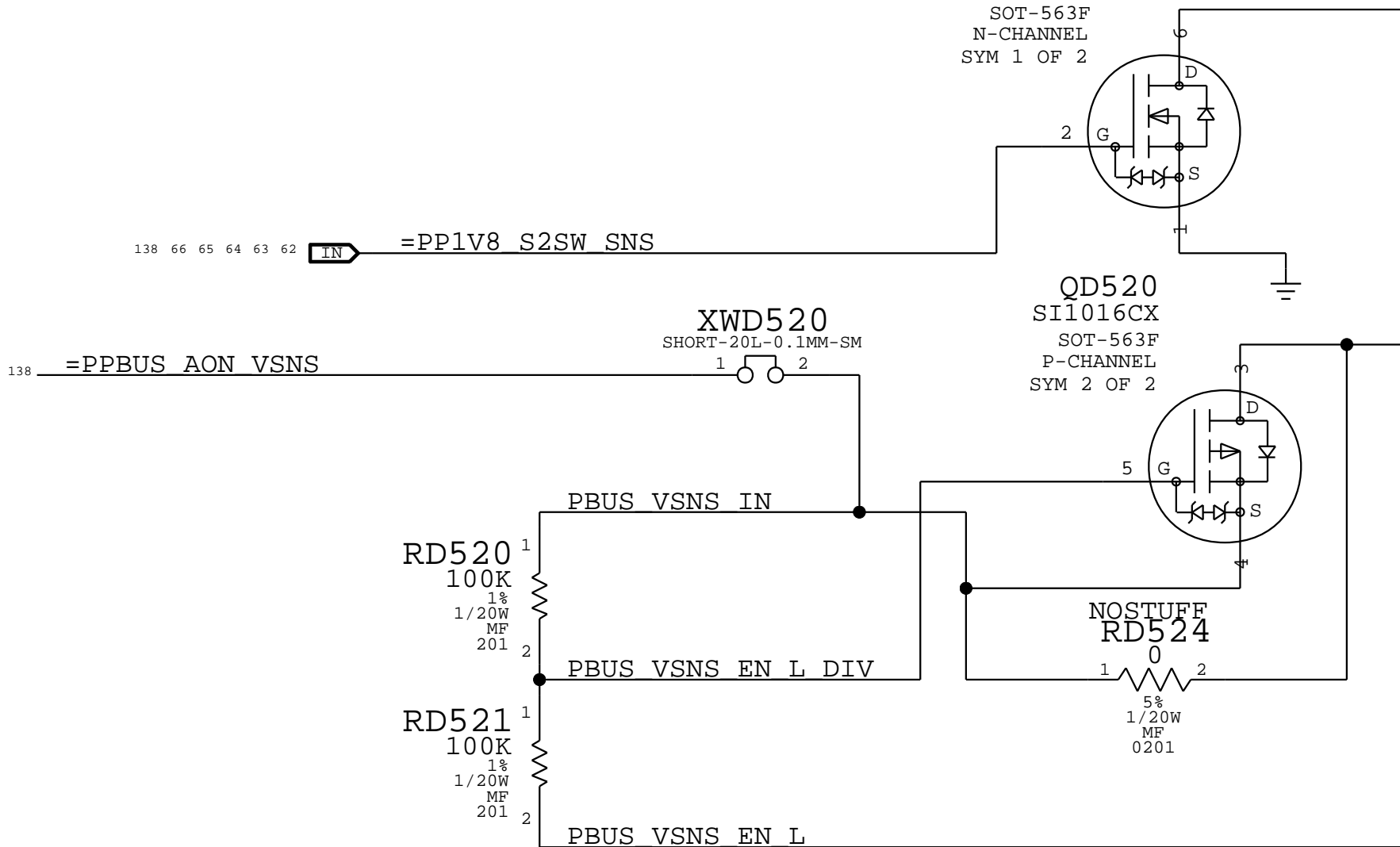
P1V8VDDH HIGH SIDE ISENSE

Gain: 100, EDP: 17.326 A
Rsense: 0.00075 Ohm
Vsense: 12.99 mV, Range: 20A
SPMU: AMUX_A0, 1ms



PBUS VOLTAGE SENSE

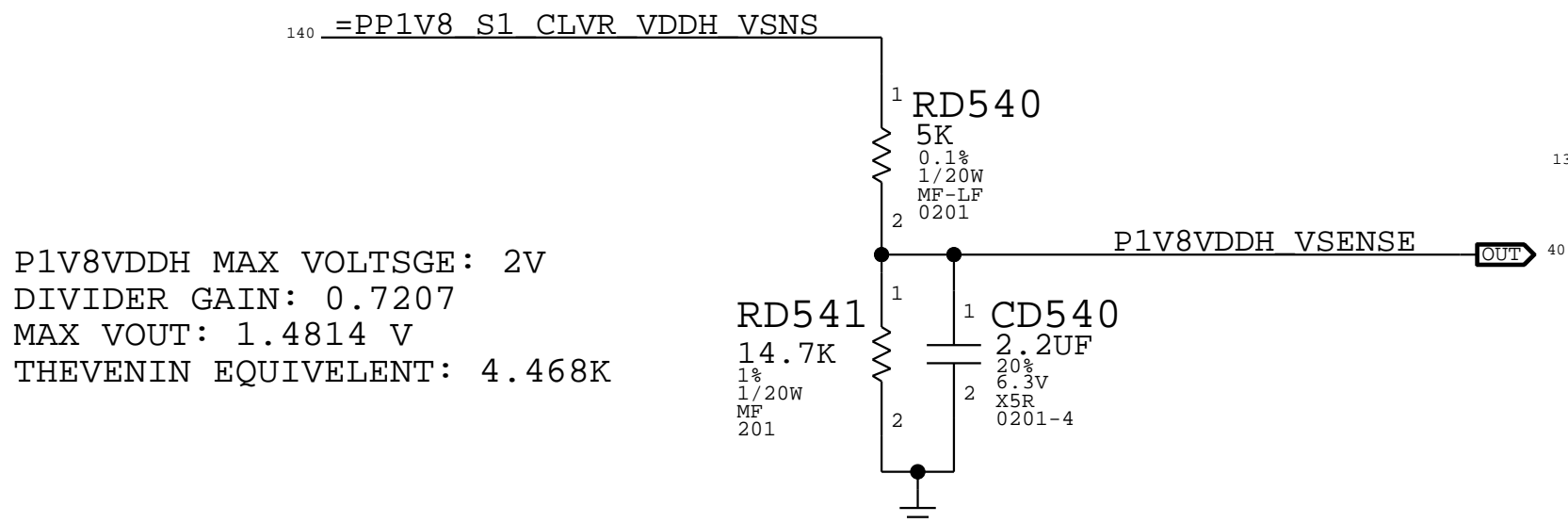
MPMU: AMUX_A3, 1ms



MAX PBUS VOLTAGE: 13.05V + 5% -> 13.7V
DIVIDER GAIN: 0.106
MAX VOUT: 1.4522
THEVENIN EQUIVELENT: 4.559K

P1V8VDDH VSENSE

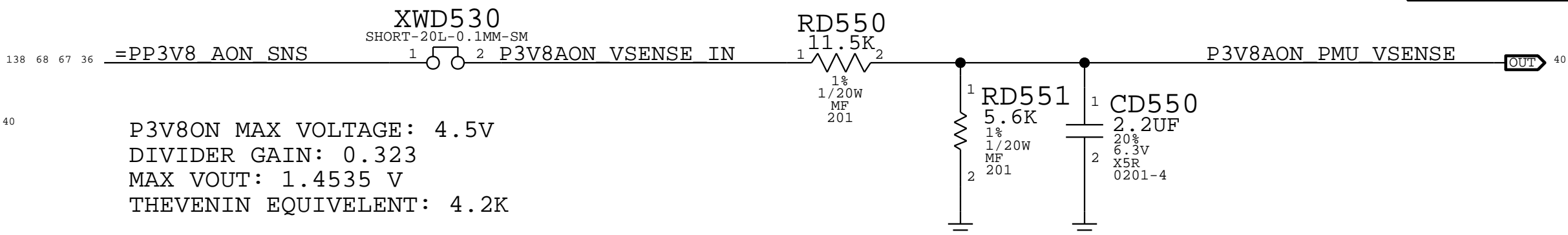
SPMU: AMUX_A1, 1ms




P1V8VDDH MAX VOLTSGE: 2V
DIVIDER GAIN: 0.7207
MAX VOUT: 1.4814 V
THEVENIN EQUIVELENT: 4.468K

P3V8AON VSENSE

SPMU: AMUX_A2, 1ms



P3V8ON MAX VOLTAGE: 4.5V
DIVIDER GAIN: 0.323
MAX VOUT: 1.4535 V
THEVENIN EQUIVELENT: 4.2K

PAGE TITLE		
SENSORS: HIGH-SIDE (1/2)		
 Apple Inc.	DRAWING NUMBER	051-06558
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	PAGE	135 OF 998
	SHEET	62 OF 156

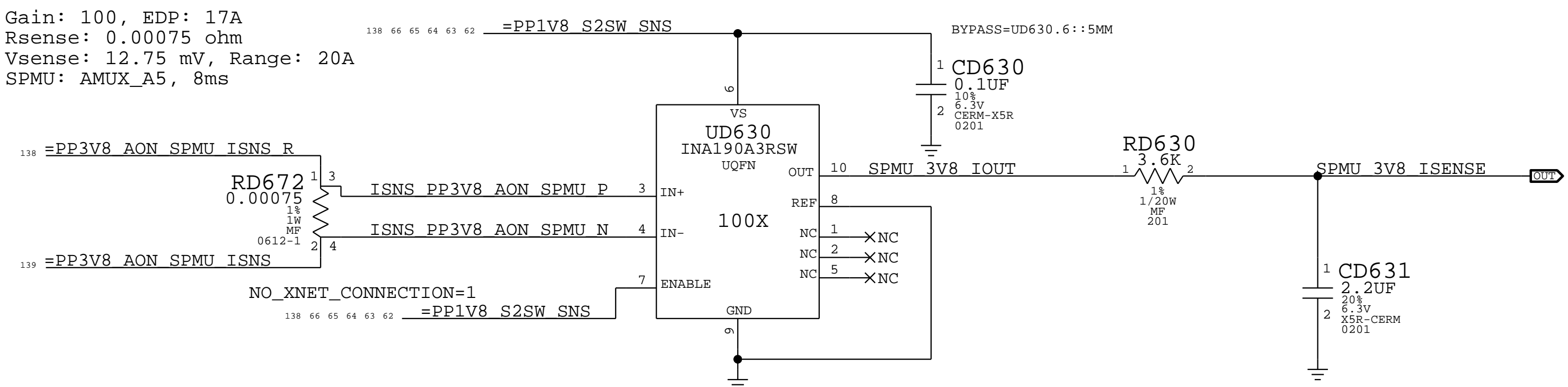
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A



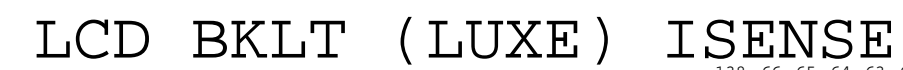
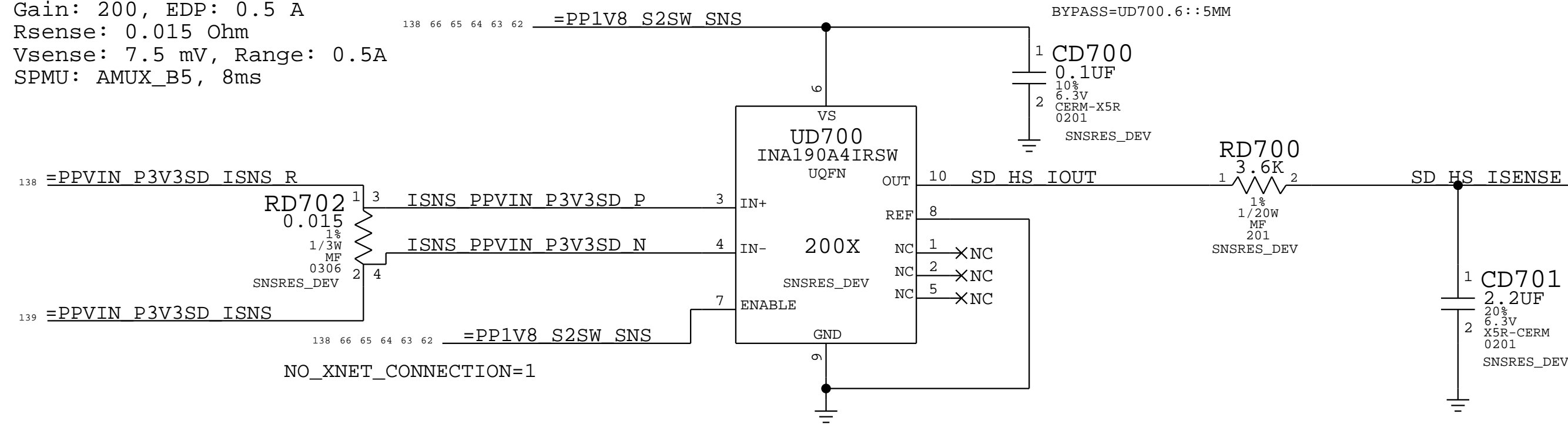
Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
SPMU: AMUX_B3, 8ms

138 ==PPBVS NAND1 ISNS_R
RD670
0.003
1/3W
MF
0306
139 ==PPBVS NAND1 ISNS
SNSRES_DEV
138 66 65 64 63 62 ==PPIV8 S2SW SNS
VS
UD650
INA190A4IRSW
UQFN
OUT 10 VCCNAND1 HS IOUT
REF 8
NO 1 XNC
2 XNC
5 XNC
7 ENABLE
GND
138 66 65 64 63 62 ==PPIV8 S2SW SNS
NO_XNET_CONNECTION=1
BYPASS=UD650.6:5MM
1 CD650
0.1UF
10V
6.3V
CERM-X5R
0201
SNSRES_DEV
RD662
3.6K
1/20W
MF
201
SNSRES_DEV
1 CD637
2.2UF
20V
6.3V
X5C-CERM
0201
SNSRES_DEV

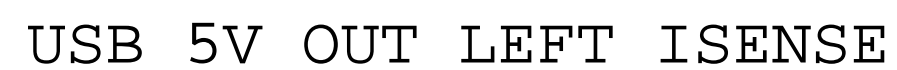
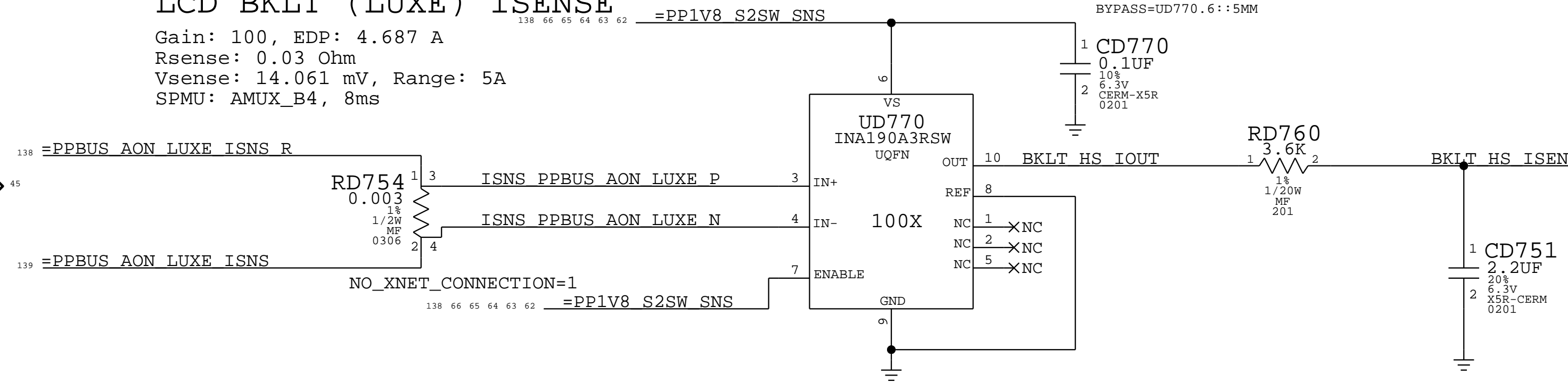
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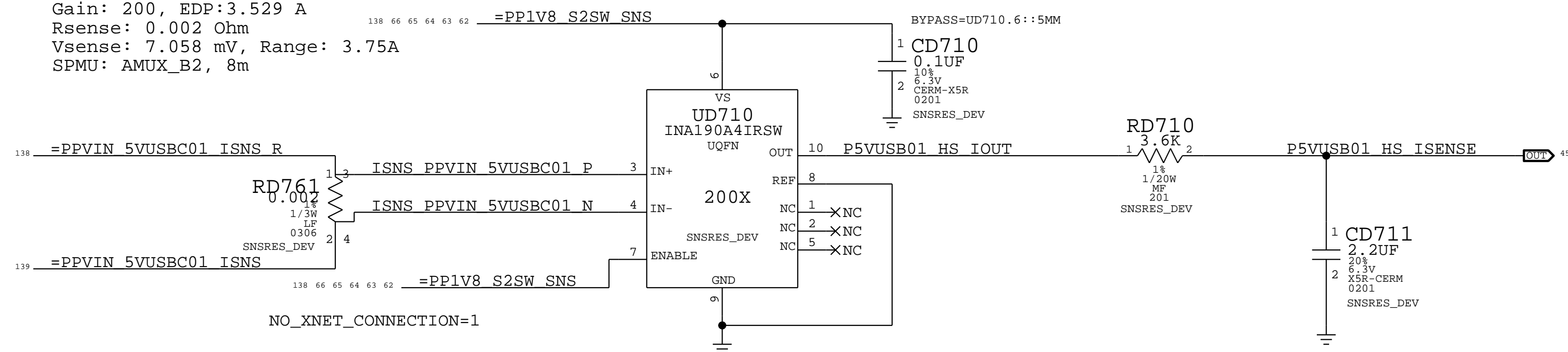
```
Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX_B5, 8ms
```



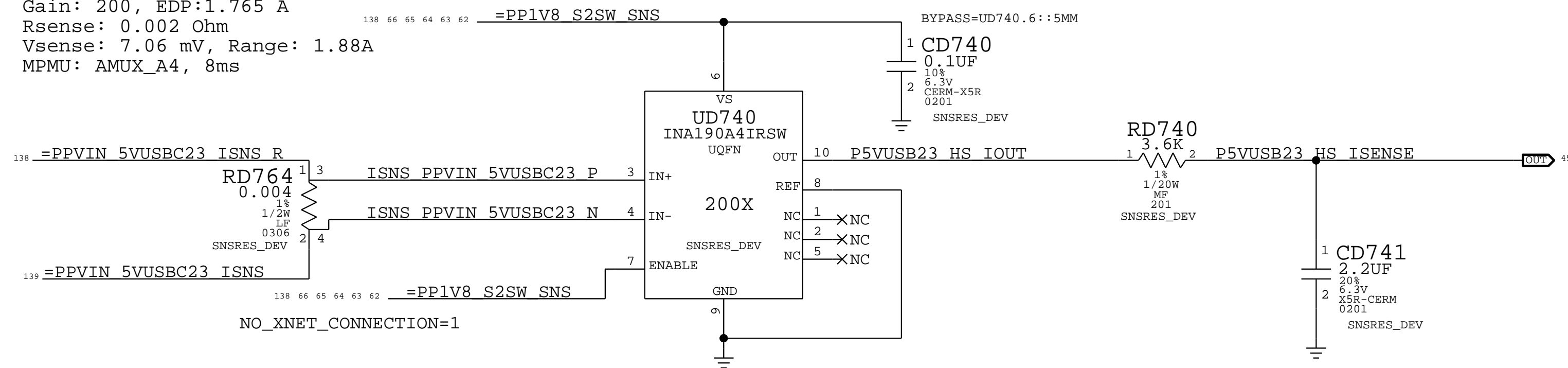
```
Gain: 100, EDP: 4.687 A
Rsense: 0.03 Ohm
Vsense: 14.061 mV, Range: 5A
SPMU: AMUX_B4, 8ms
```



```
Gain: 200, EDP:3.529 A
Rsense: 0.002 Ohm
Vsense: 7.058 mV, Range: 3.75A
SPMU: AMUX_B2, 8m
```



```
Gain: 200, EDP:1.765 A
Rsense: 0.002 Ohm
Vsense: 7.06 mV, Range: 1.88A
MPMU: AMUX_A4, 8ms
```



D

C

B

A


D

C

B

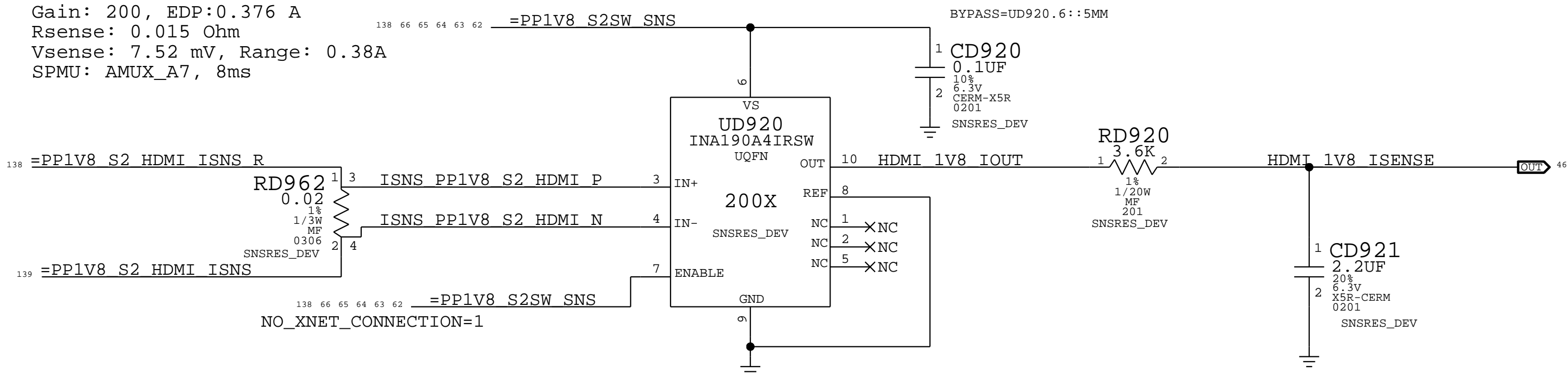
A

BOM_COST_GROUP=SENSORS

PAGE TITLE		SENSORS: LOW-SIDE (1/3)	
 Apple Inc.	DRAWING NUMBER	051-06558	SIZE D
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		SHEET 65 OF 156	

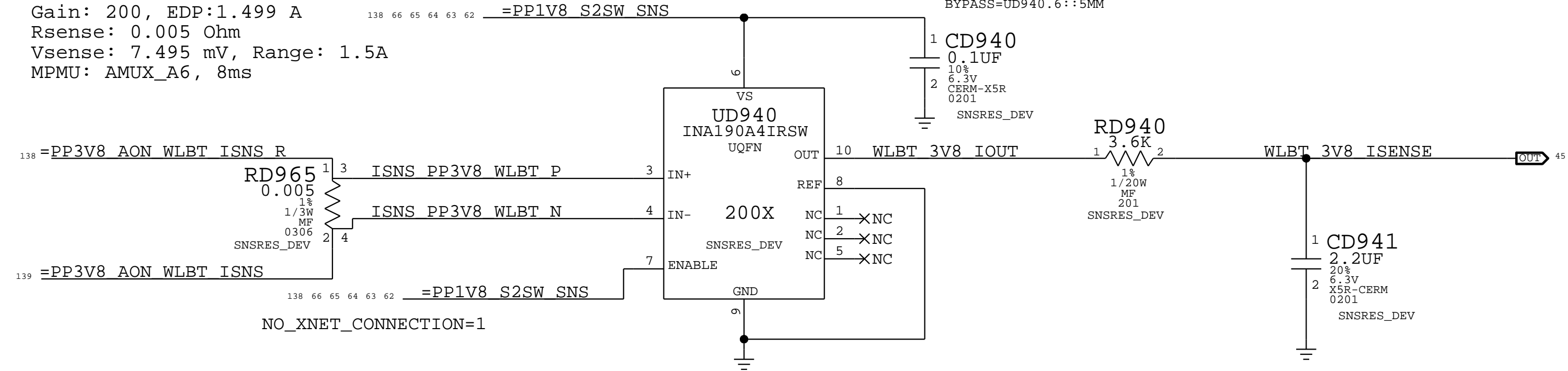
HDMI 1V8 ISENSE

Gain: 200, EDP:0.376 A
Rsense: 0.015 Ohm
Vsense: 7.52 mV, Range: 0.38A
SPMU: AMUX_A7, 8ms



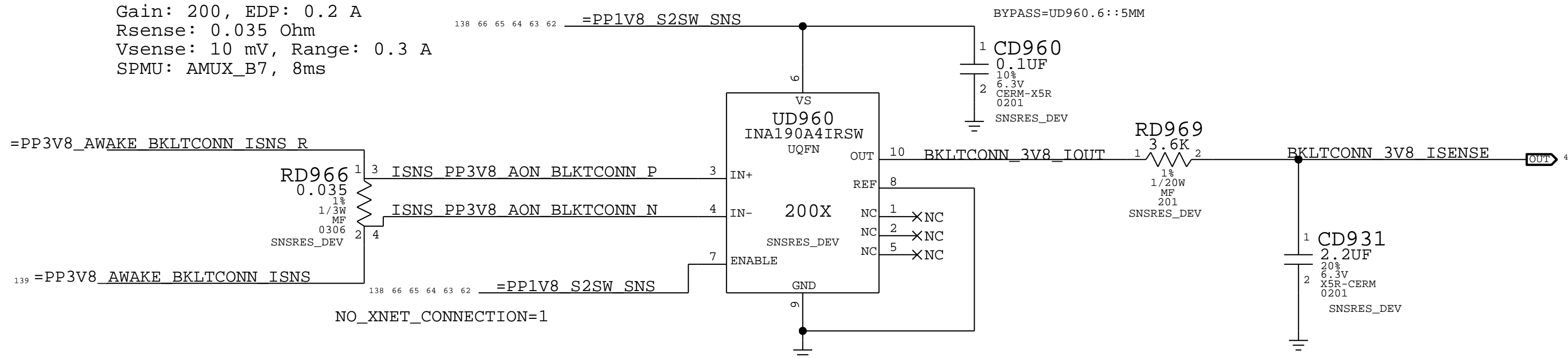
WLAN BT 3V8 ISENSE

Gain: 200, EDP:1.499 A
Rsense: 0.005 Ohm
Vsense: 7.495 mV, Range: 1.5A
MPMU: AMUX_A6, 8ms



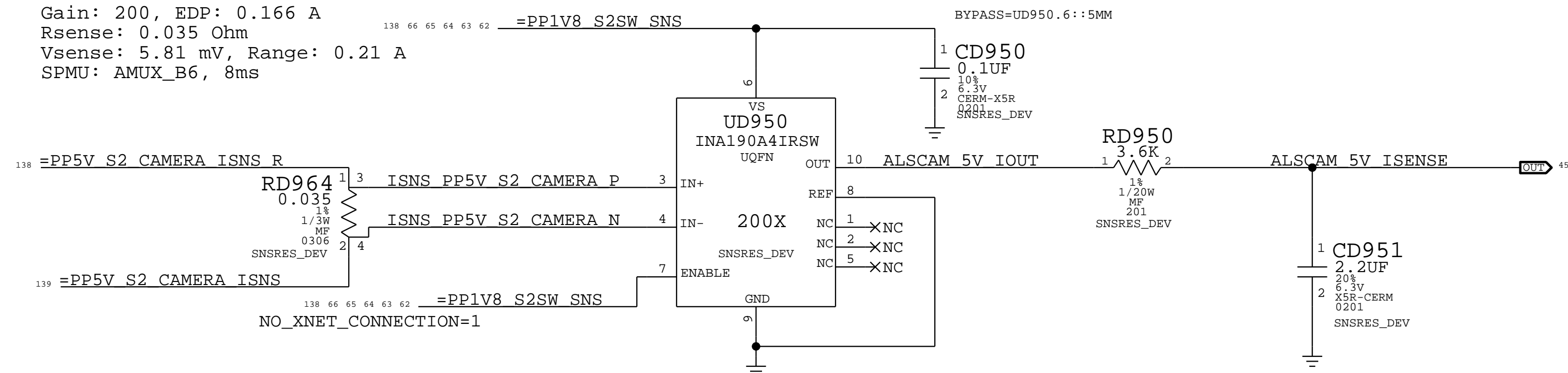
DISPLAY BACKLIGHT 3V8 ISENSE

Gain: 200, EDP: 0.2 A
Rsense: 0.035 Ohm
Vsense: 10 mV, Range: 0.3 A
SPMU: AMUX_B7, 8ms



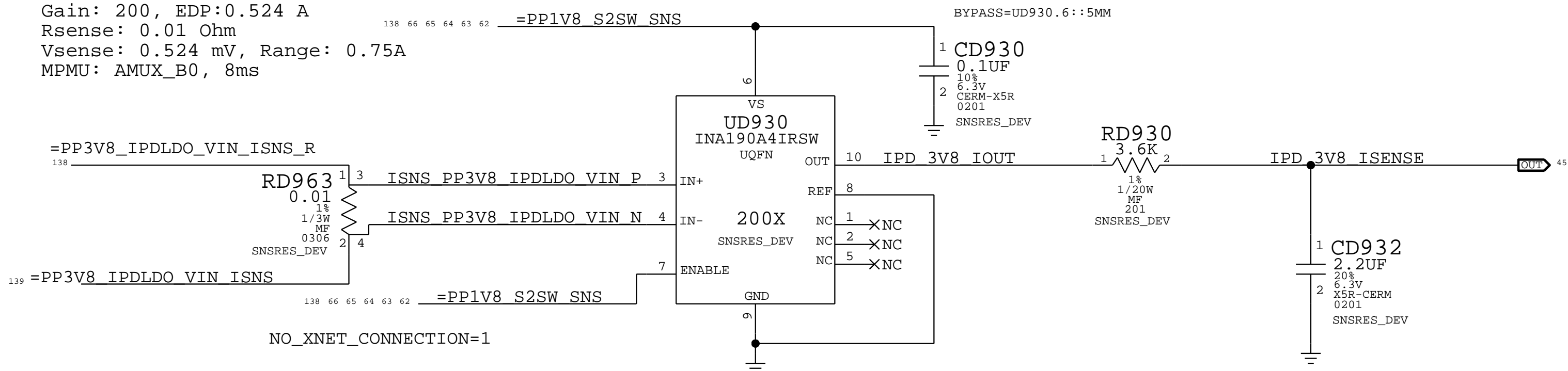
CAMERA 5V ISENSE

Gain: 200, EDP: 0.166 A
Rsense: 0.035 Ohm
Vsense: 5.81 mV, Range: 0.21 A
SPMU: AMUX_B6, 8ms



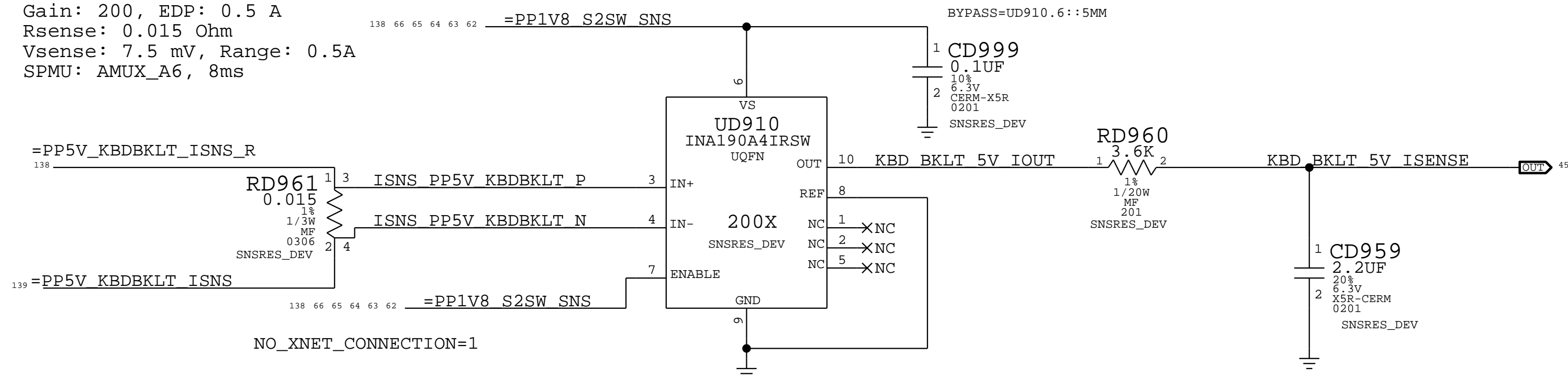
IPD 3V8 ISENSE

Gain: 200, EDP:0.524 A
Rsense: 0.01 Ohm
Vsense: 0.524 mV, Range: 0.75A
MPMU: AMUX_B0, 8ms



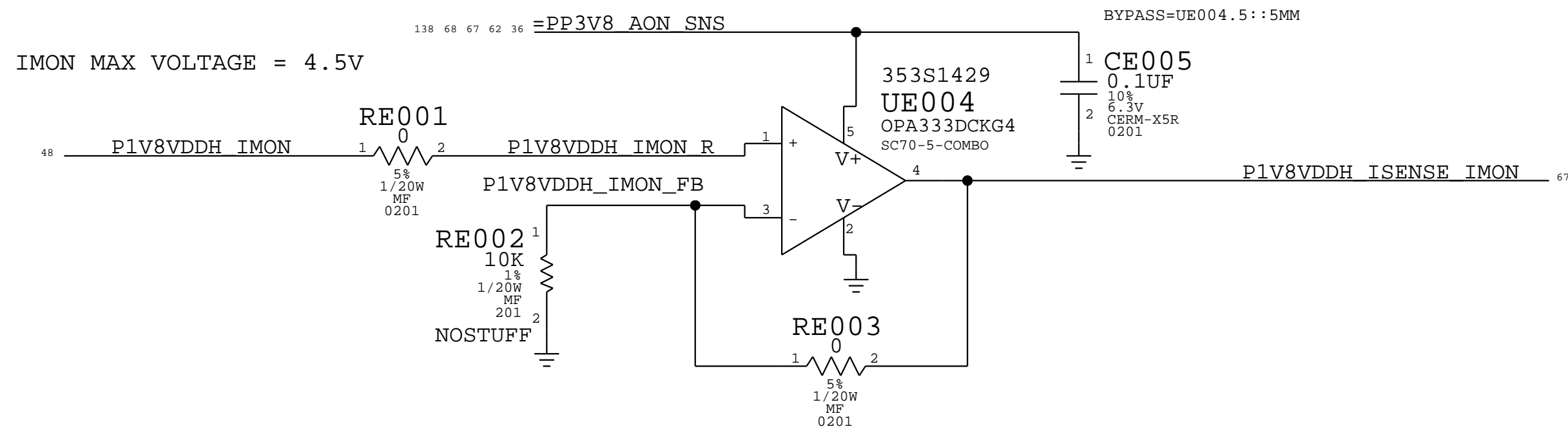
KBD BACKLIGHT ISENSE

Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX_A6, 8ms



PAGE TITLE		
SENSORS: LOW-SIDE (2/3)		
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	PAGE	139 OF 998
	SHEET	66 OF 156

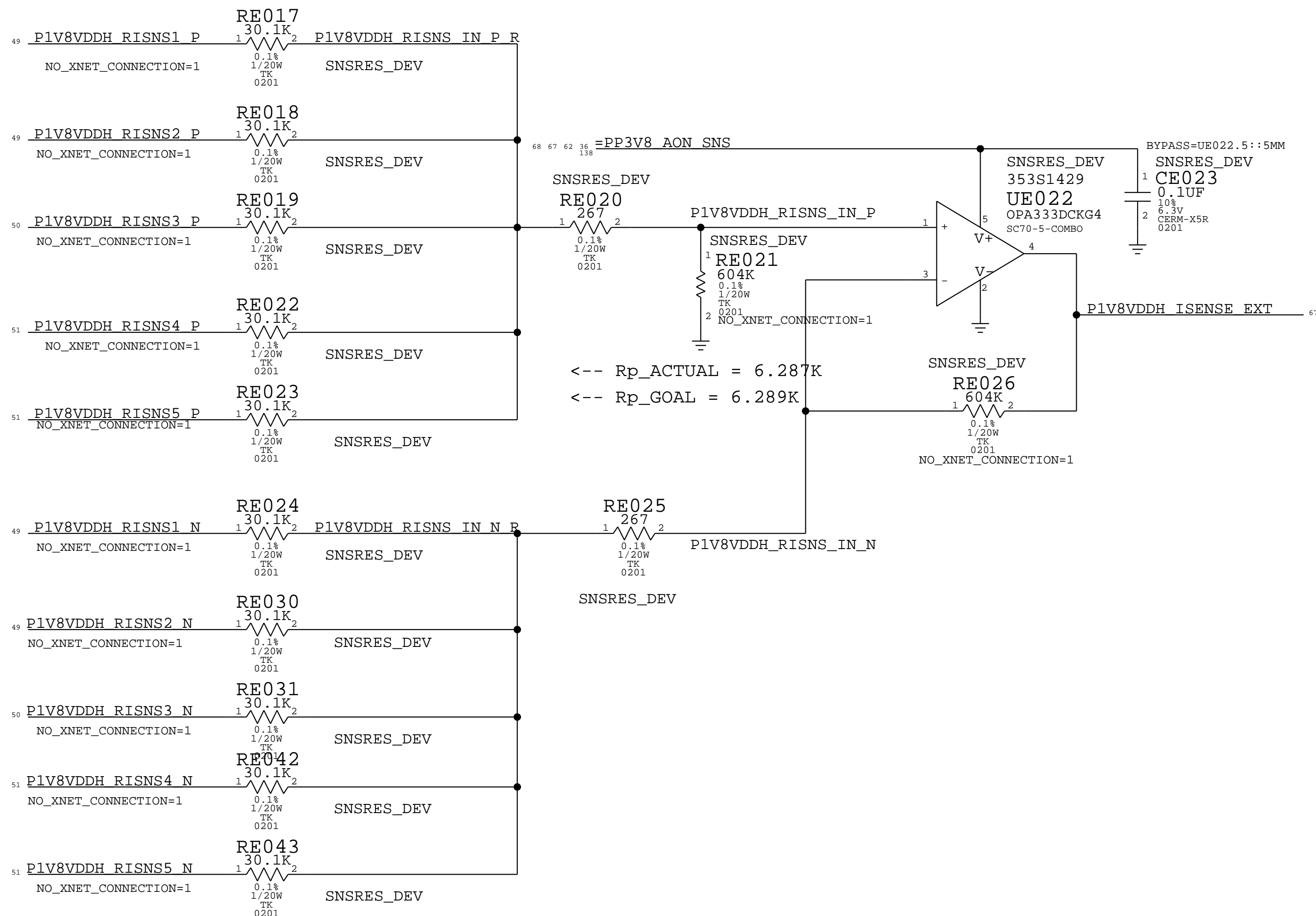
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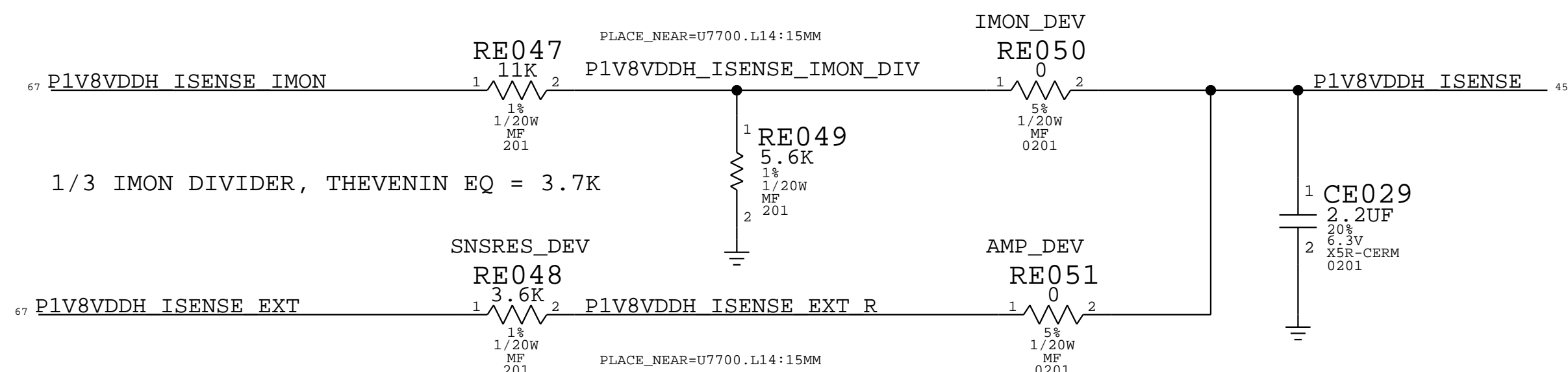
P1V8VDDH LOW SIDE ISENSE (SUMMING AMP FOR 3 PHASES)

EDP: 156.2A, 32.24A/PHASE

```
SPMU AMUX_A7, 8ms
```

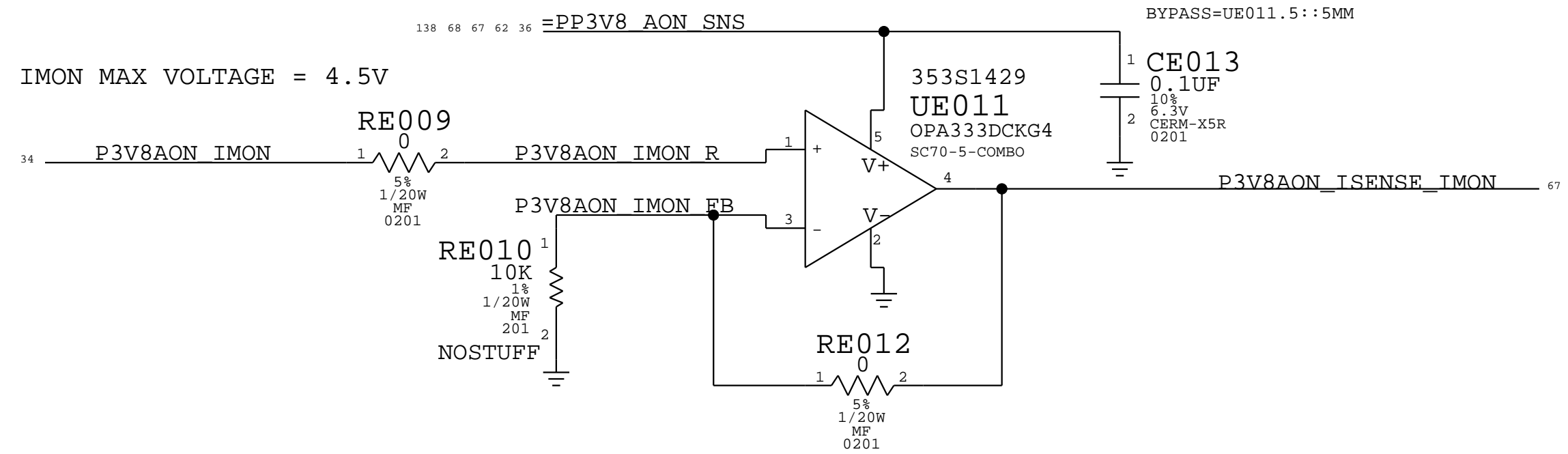


RESISTOR STUFFING OPTION FOR IMON OR SUMMING AMP



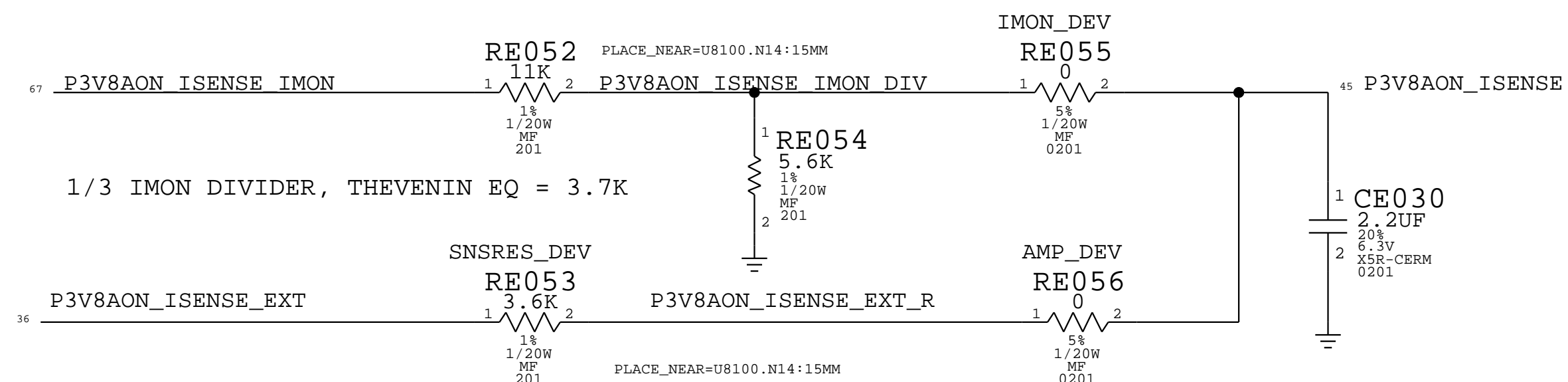
P3V8 LOW SIDE ISENSE (IMON)

SPMU AMUX_A7, 8ms, VMAX AFTER DIVIDER = 1.51V



[[P3V8 LOW SIDE ISENSE AND ILIMIT moved to CSA140]]

RESISTOR STUFFING OPTION FOR IMON OR SUMMING AMP



SENSORS: LOW-SIDE (3/3)



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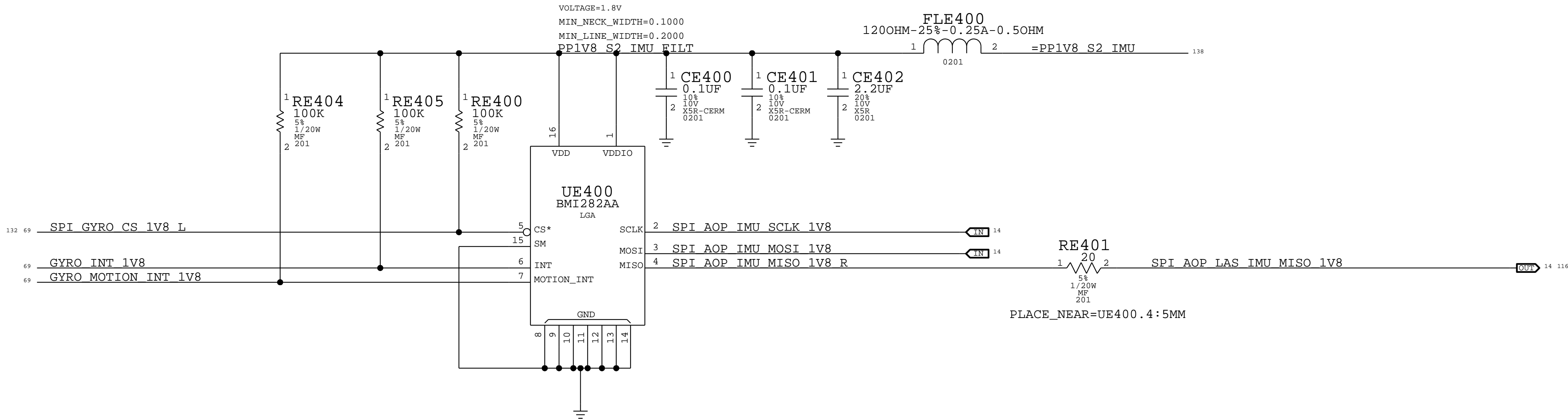
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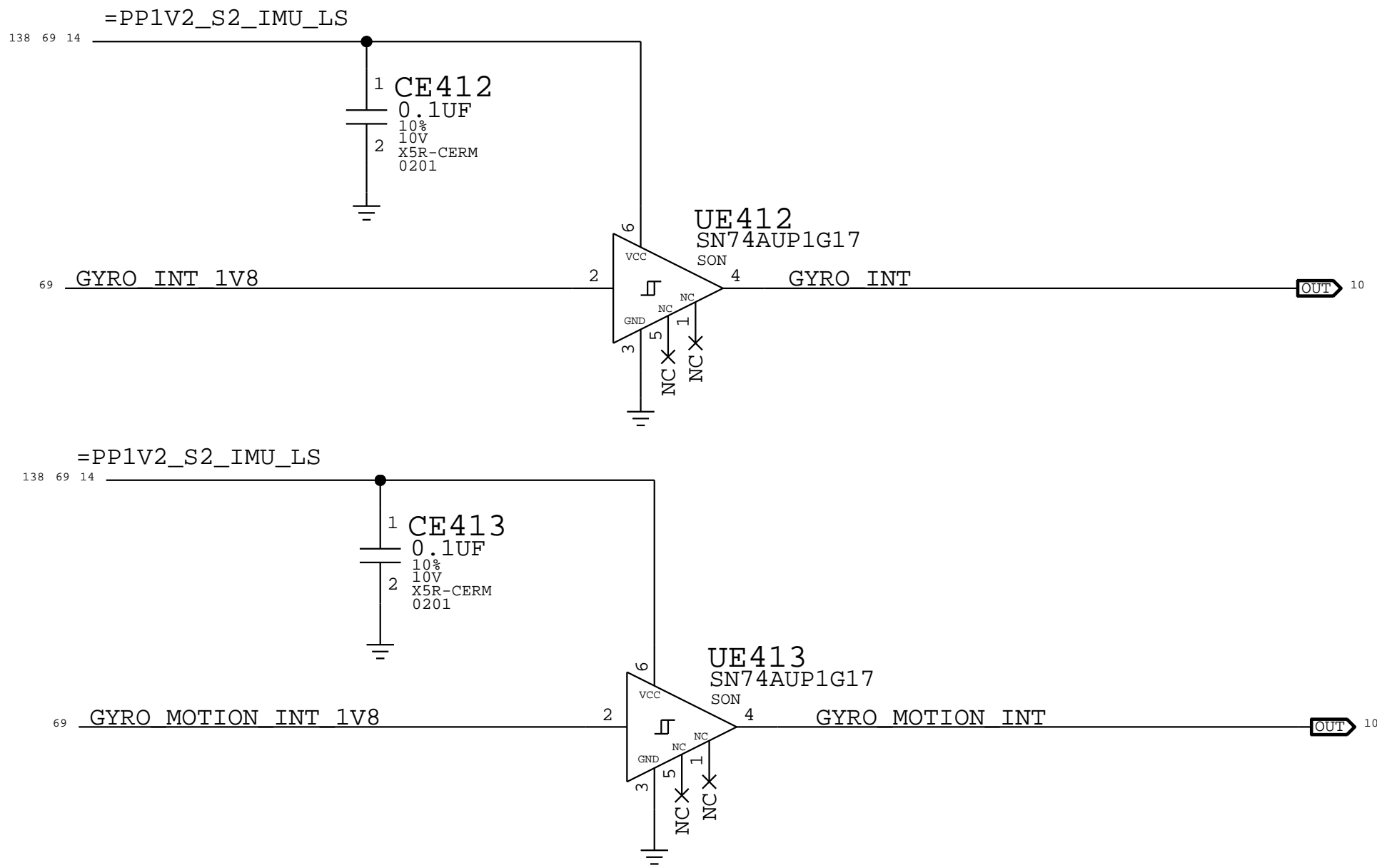
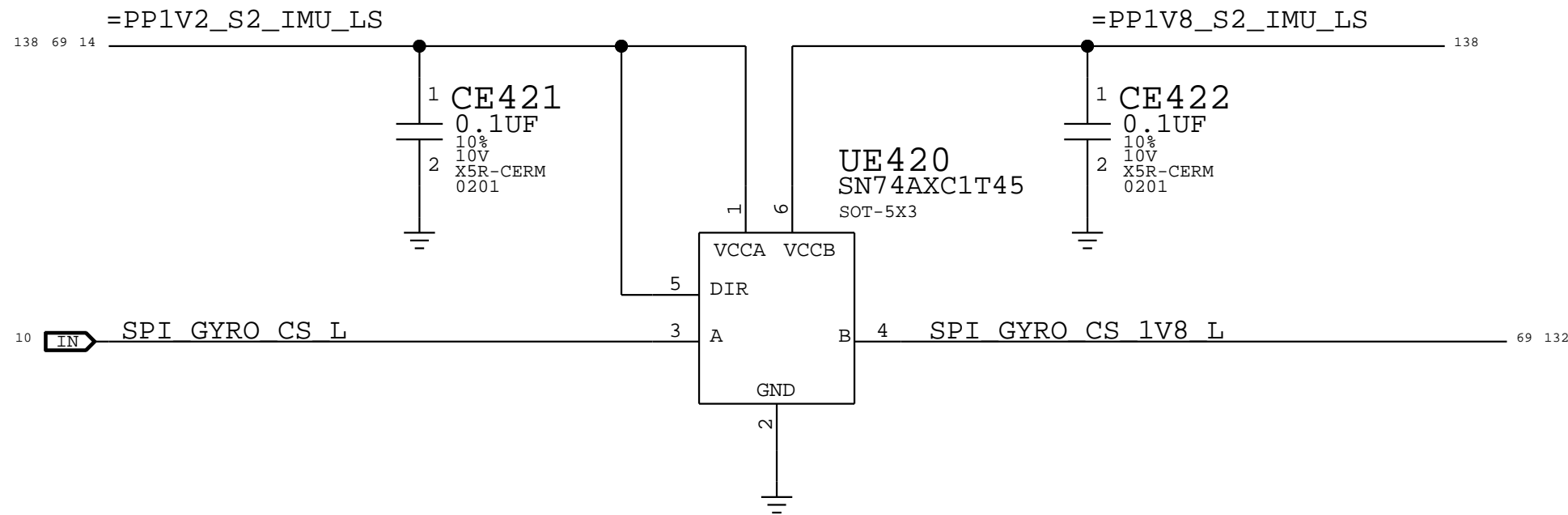
BRANCH
PAGE 140 OF 998
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KOBOL: ACCEL & GYRO

FERRITE IS PLACEHOLDER ONLY
J417 USES 1555S0686 (01005)
MUST FIND PROPER PART, IF ONE IS NEEDED AT ALL

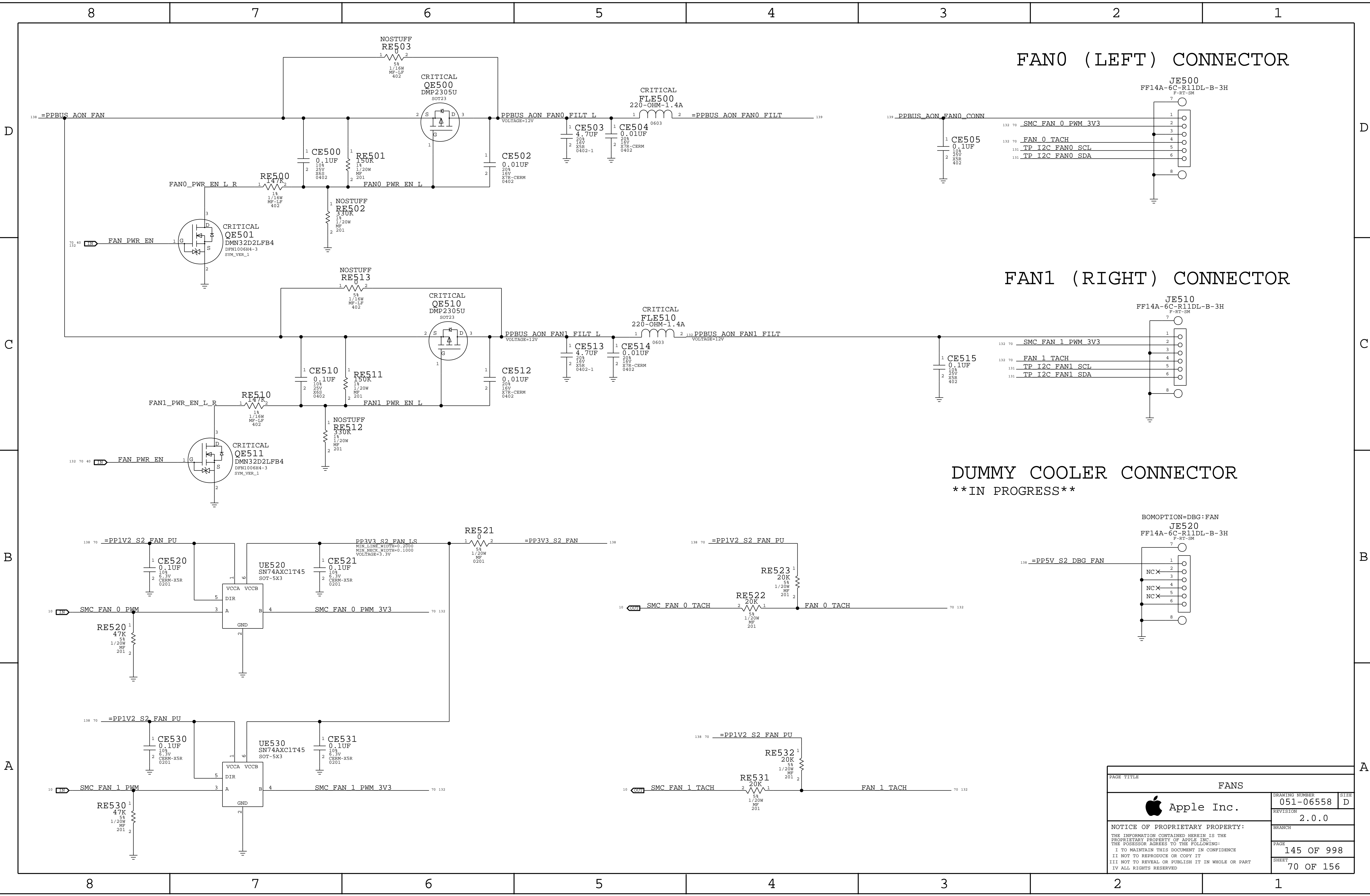


SPI LEVEL TRANSLATION



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	PAGE	144 OF 998
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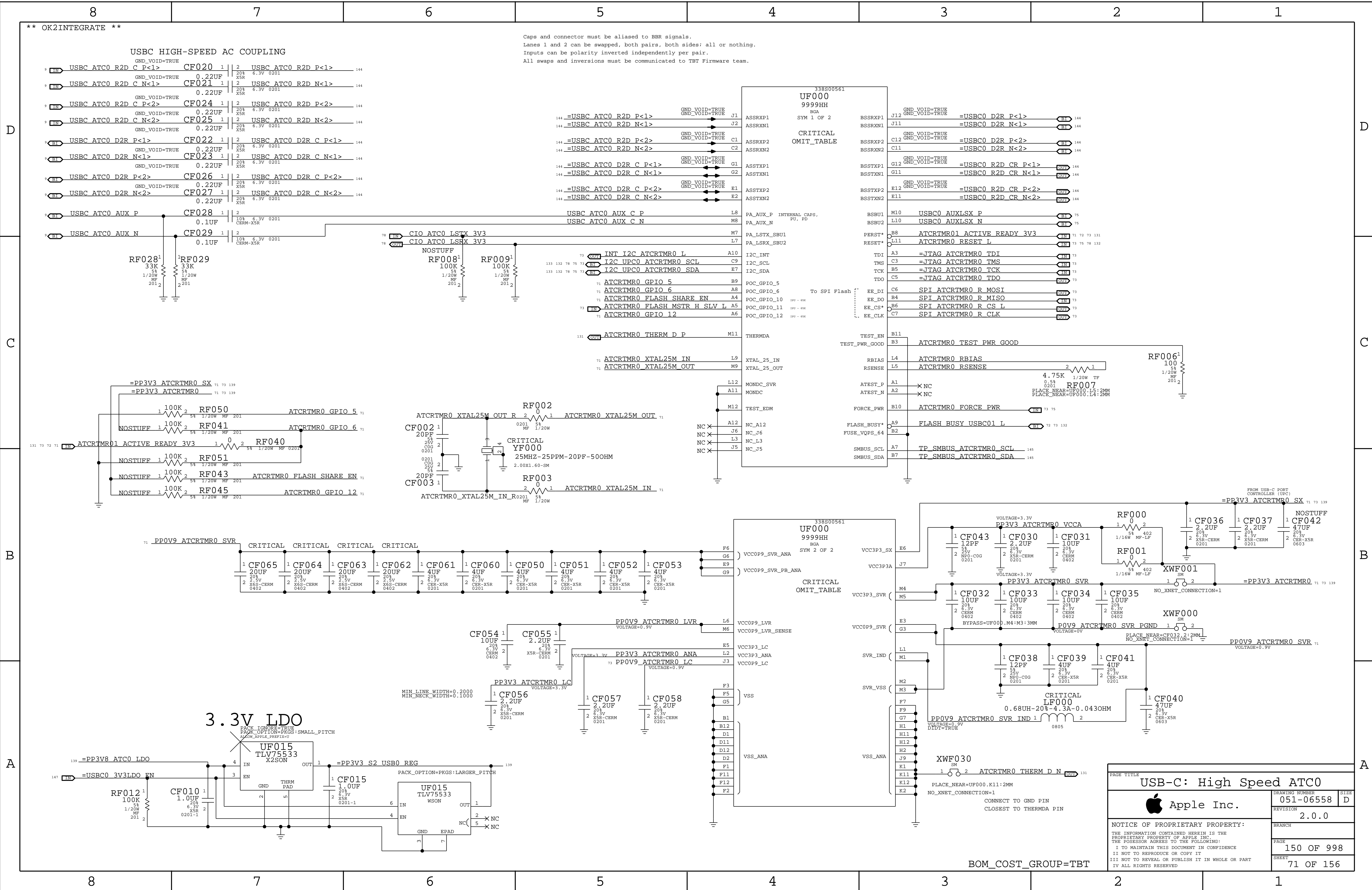


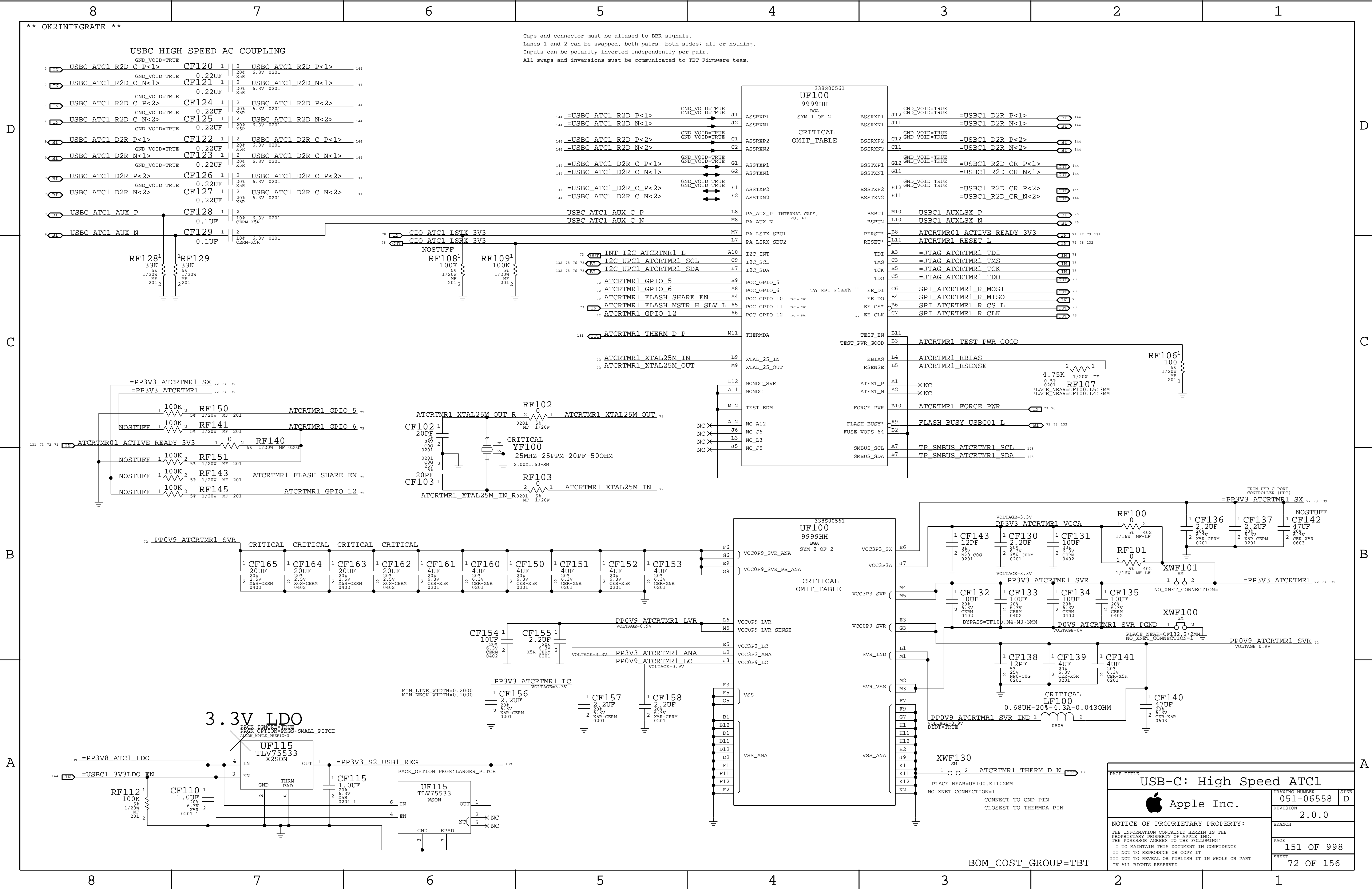
FAN0 (LEFT) CONNECTOR

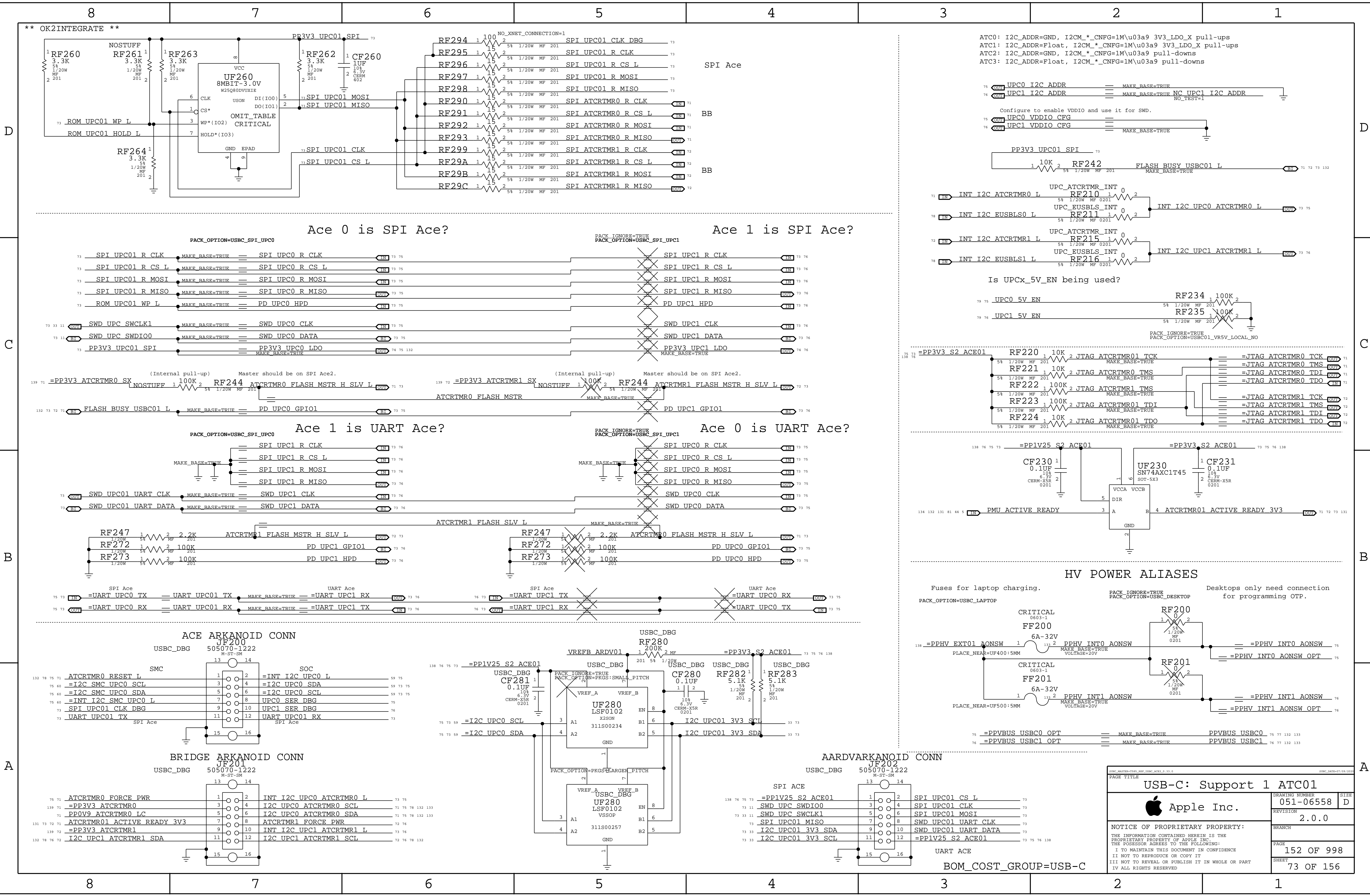
FAN1 (RIGHT) CONNECTOR


DUMMY COOLER CONNECTOR
IN PROGRESS

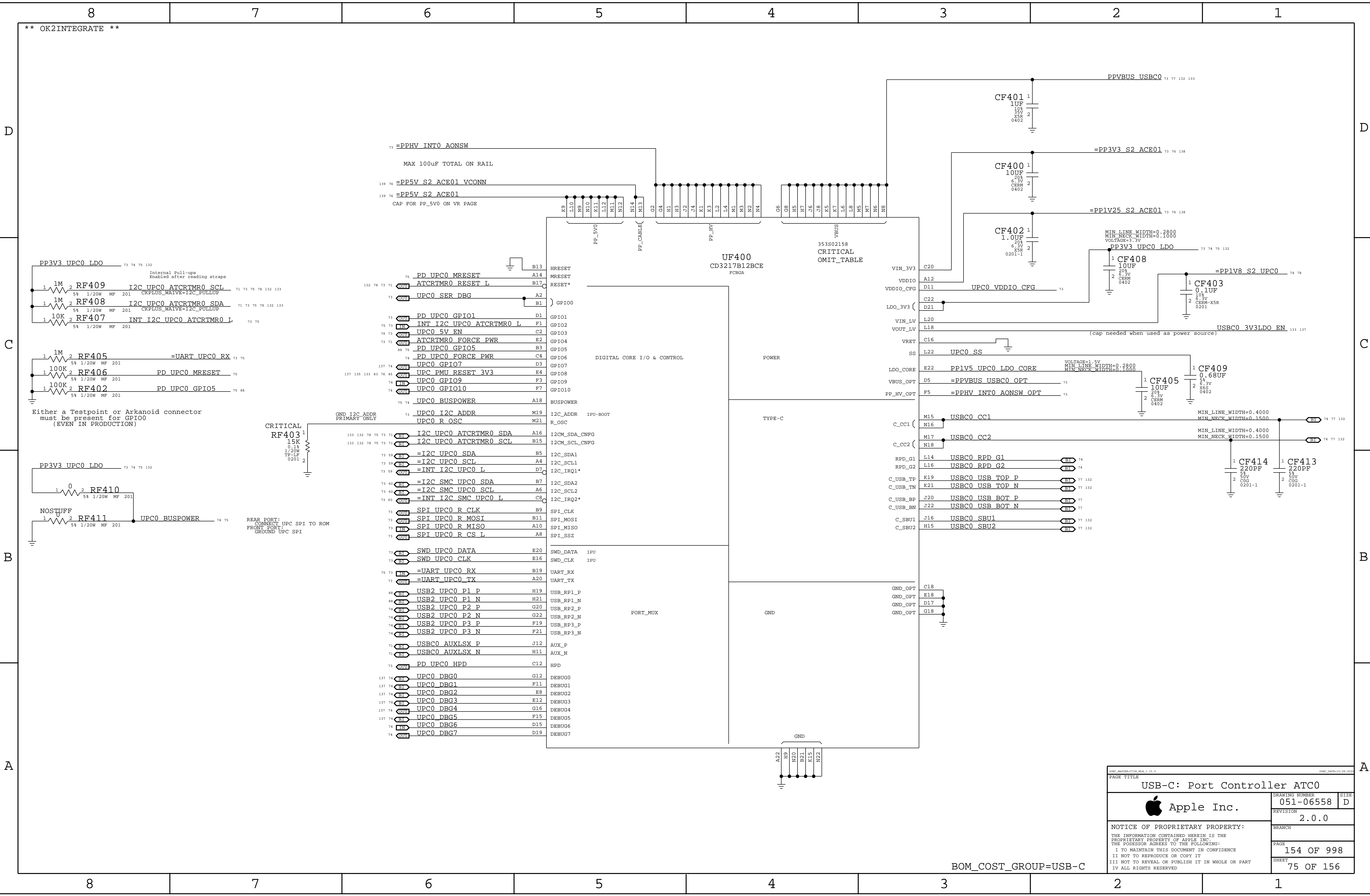
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FANS			
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	SHEET	70 OF 156	



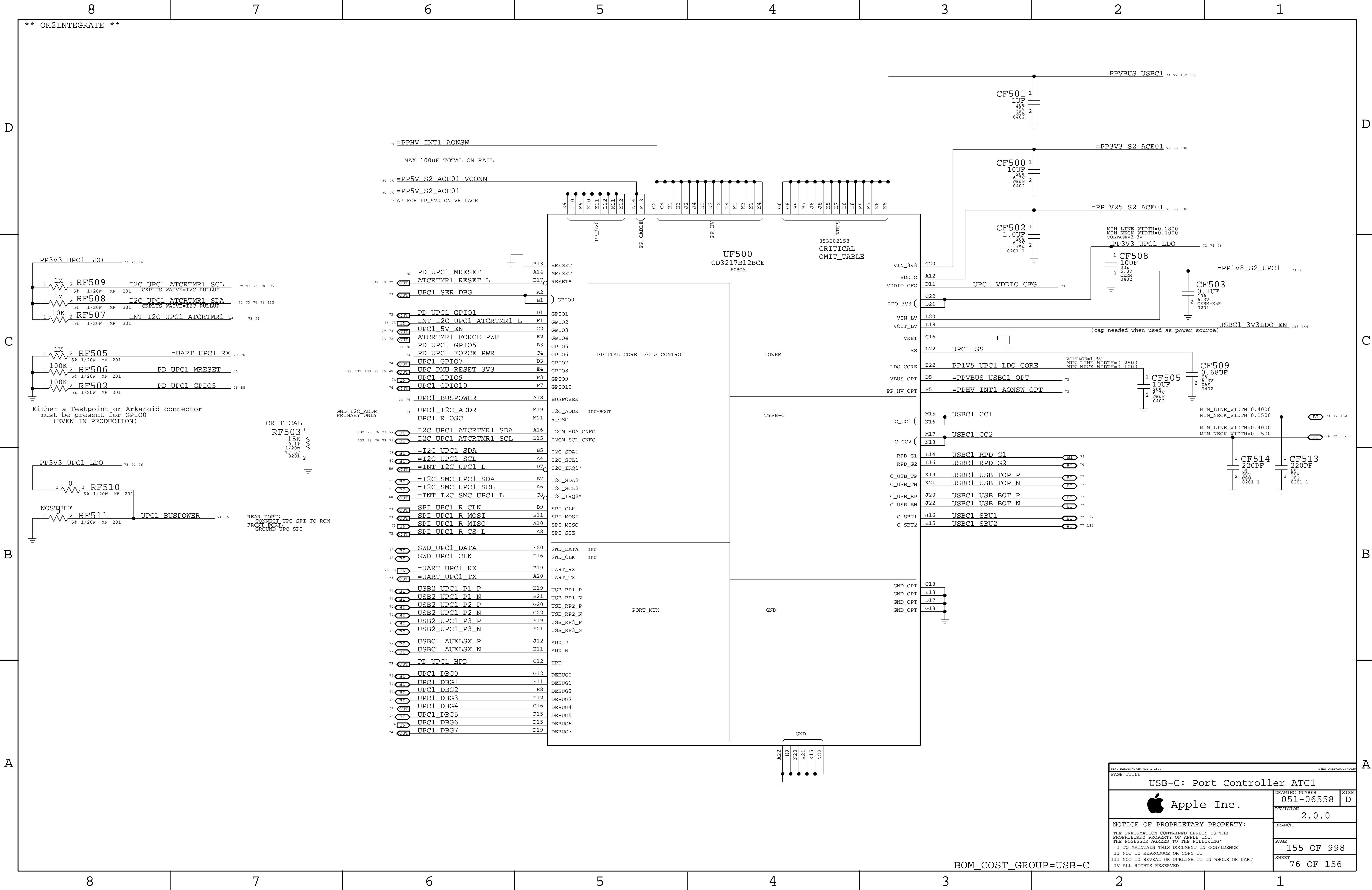




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USB-C: Support 1 ATC01		
 Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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REVISION			2.0.0					
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PAGE TITLE		DRAWING NUMBER		SIZE	
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REVISION		2.0.0			
BRANCH					
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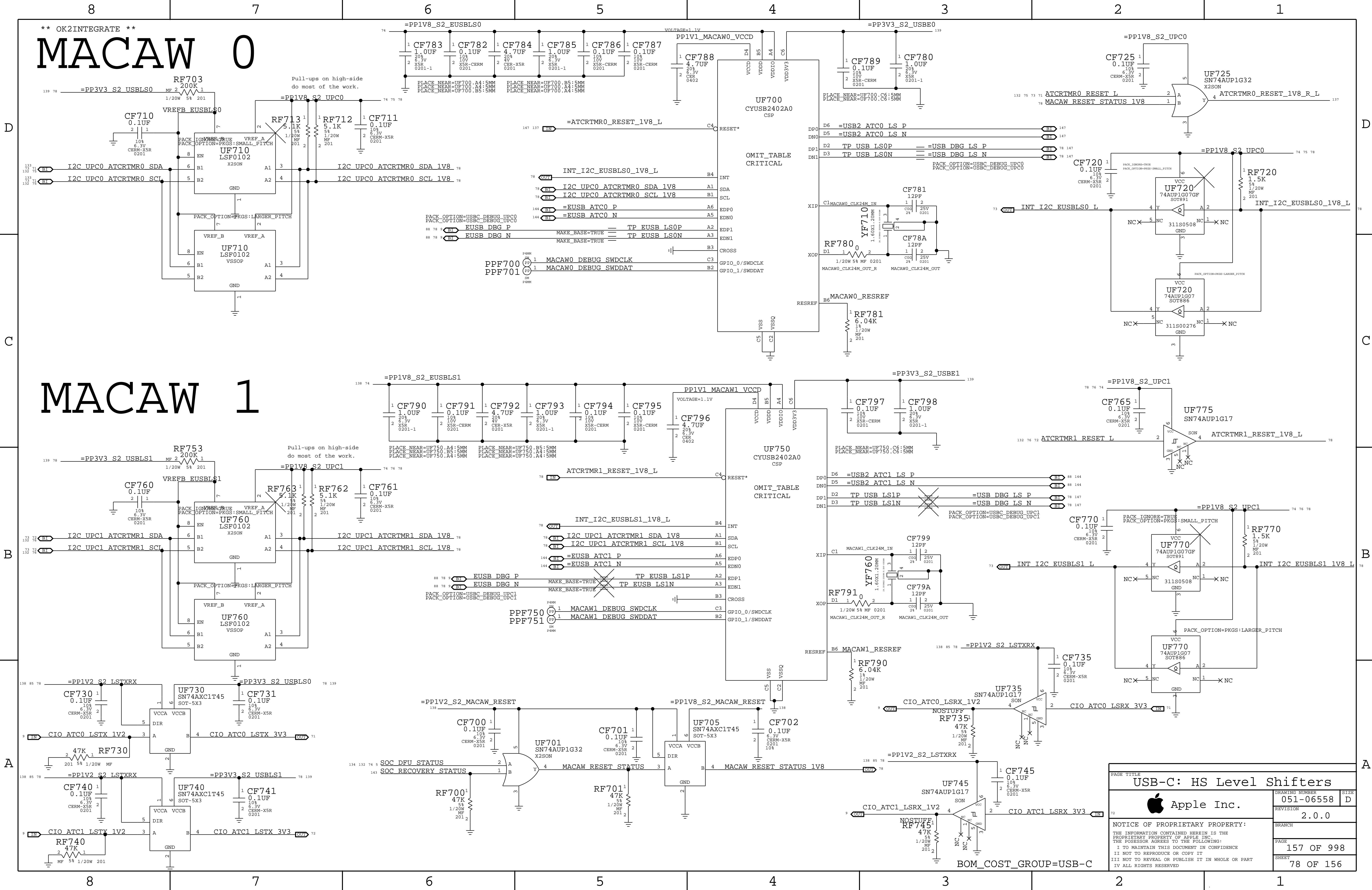
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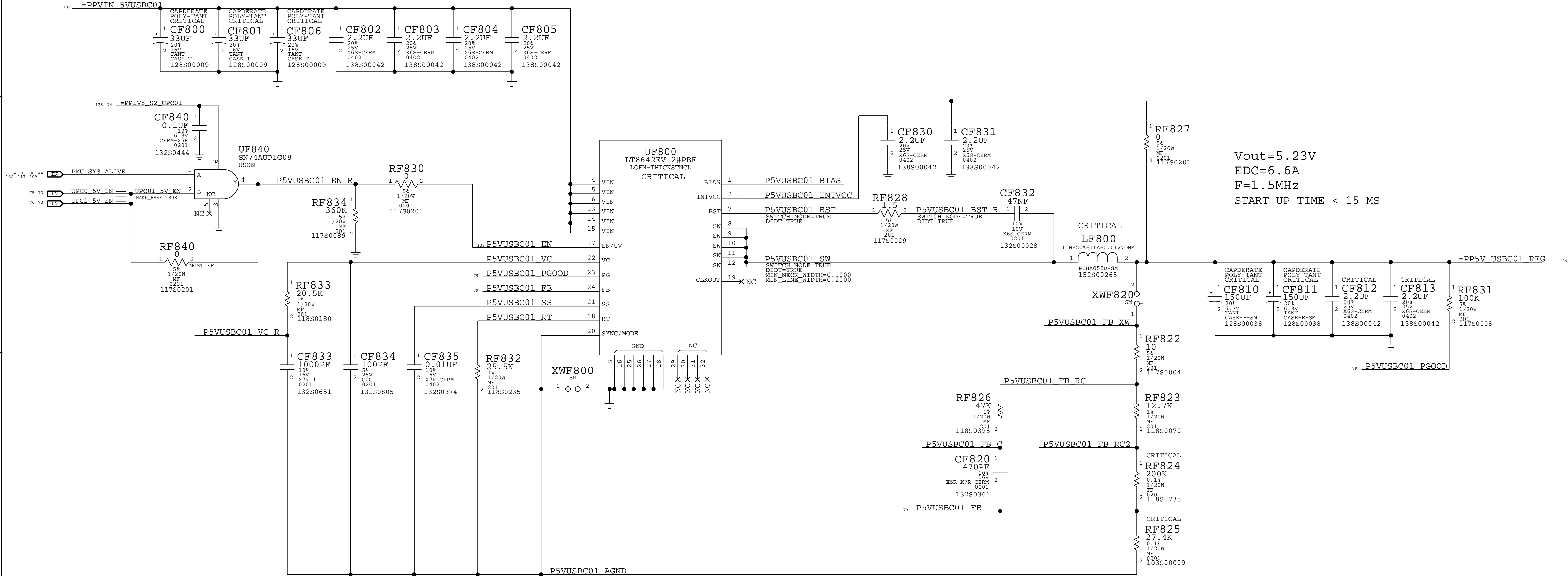
PAGE TITLE			
USB-C: Left Connectors			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-06558		D
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	2.0.0		
	BRANCH		
	PAGE		
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MACAW 1




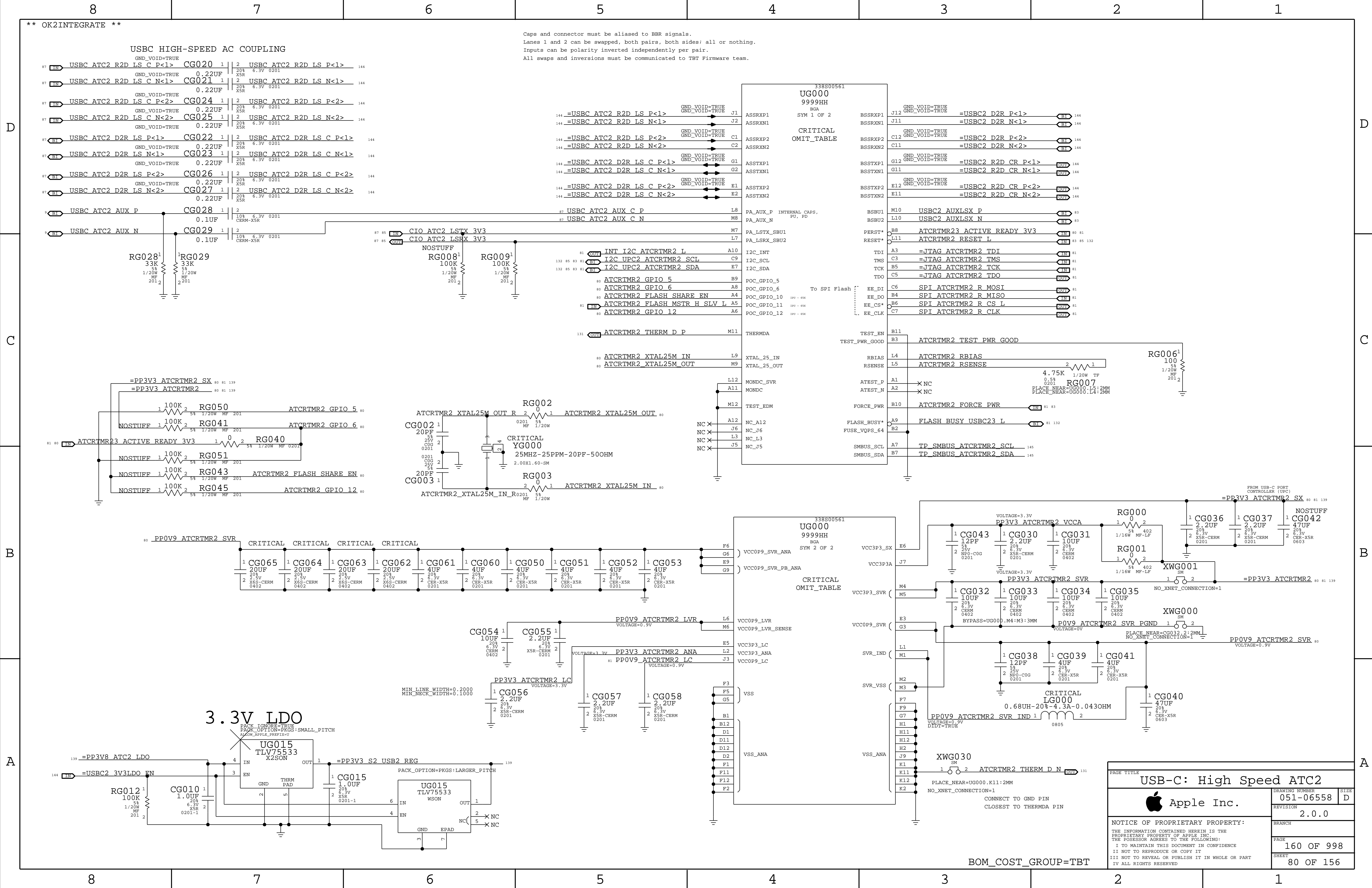
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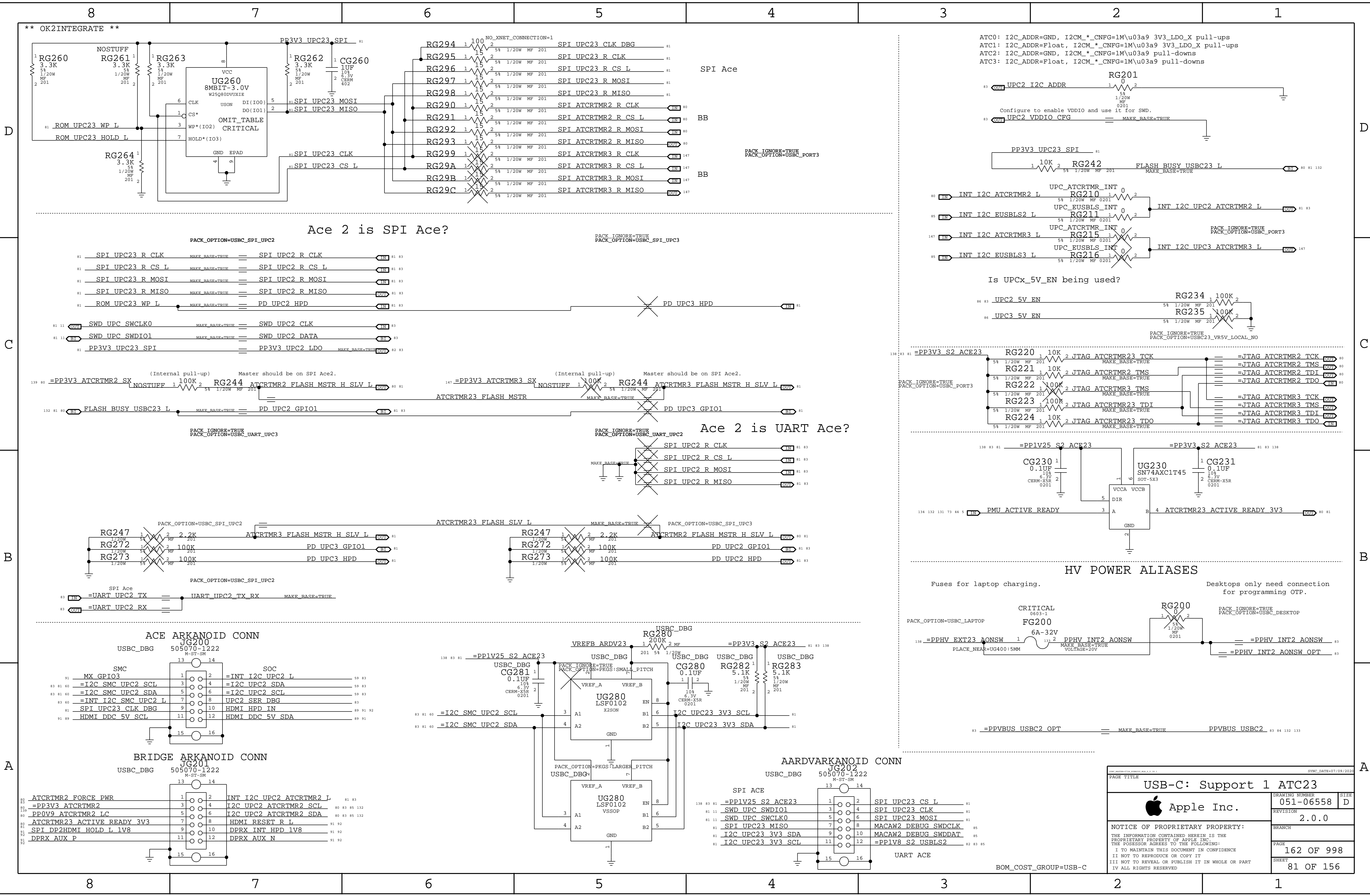


Vout=5.23V
EDC=6.6A
F=1.5MHz
START UP TIME < 15 MS

BOM_COST_GROUP=USB-C

PAGE TITLE		
USB-C: 5V Regulator		
 Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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	PAGE	158 OF 998
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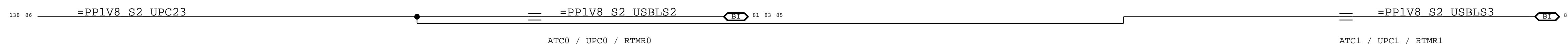


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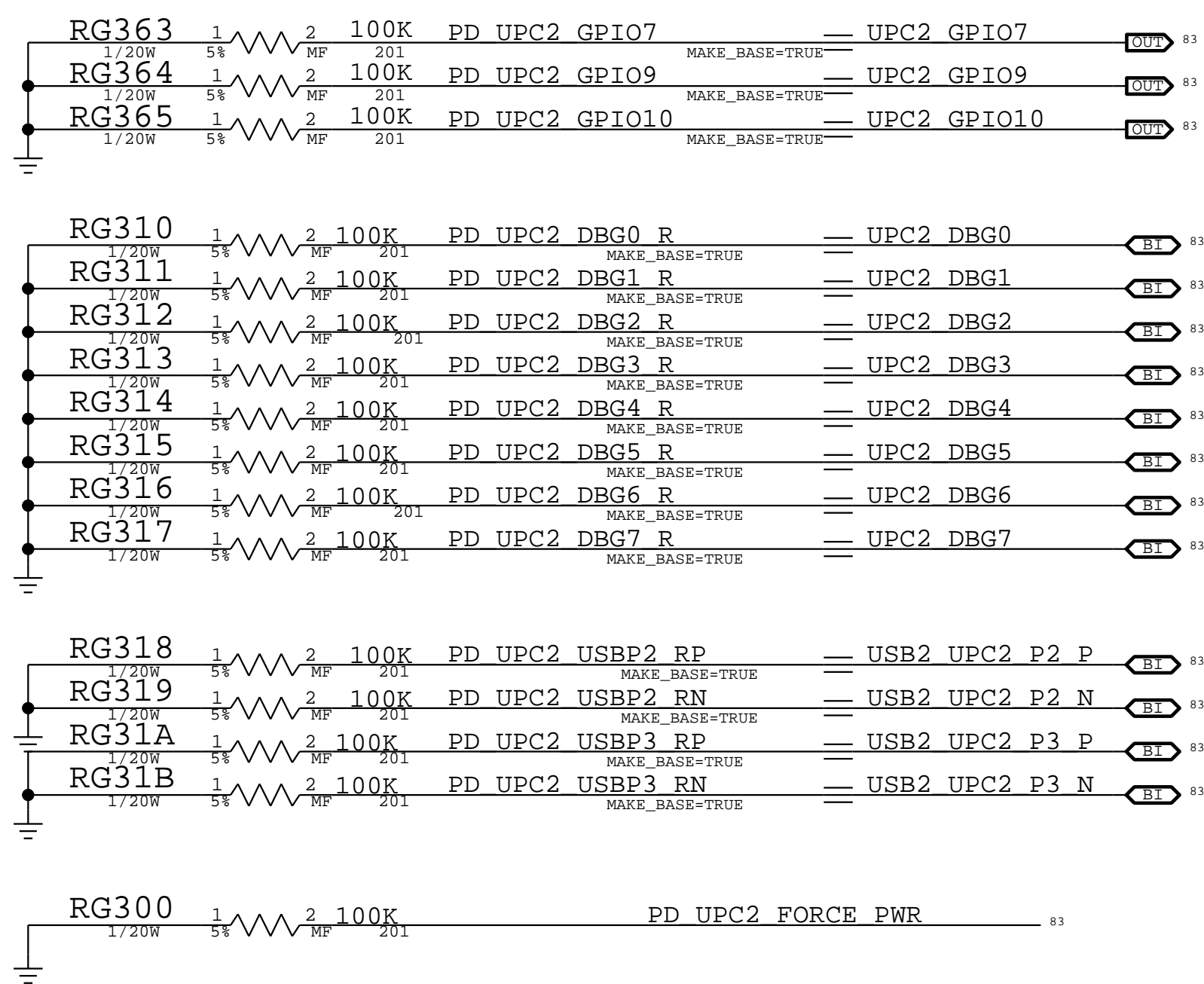
USB-C Port assignments

This schematic not currently set up to allow ATC channels 2 or 3 be the debug port. These options can be added if needed.

Unused ports

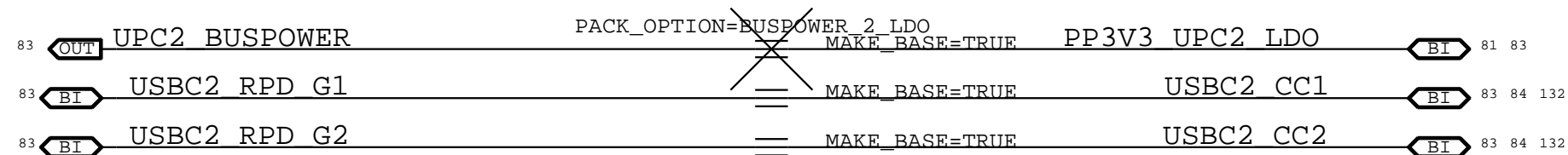


Ace2 GPIOs



Connections for Laptops (USBC power in)

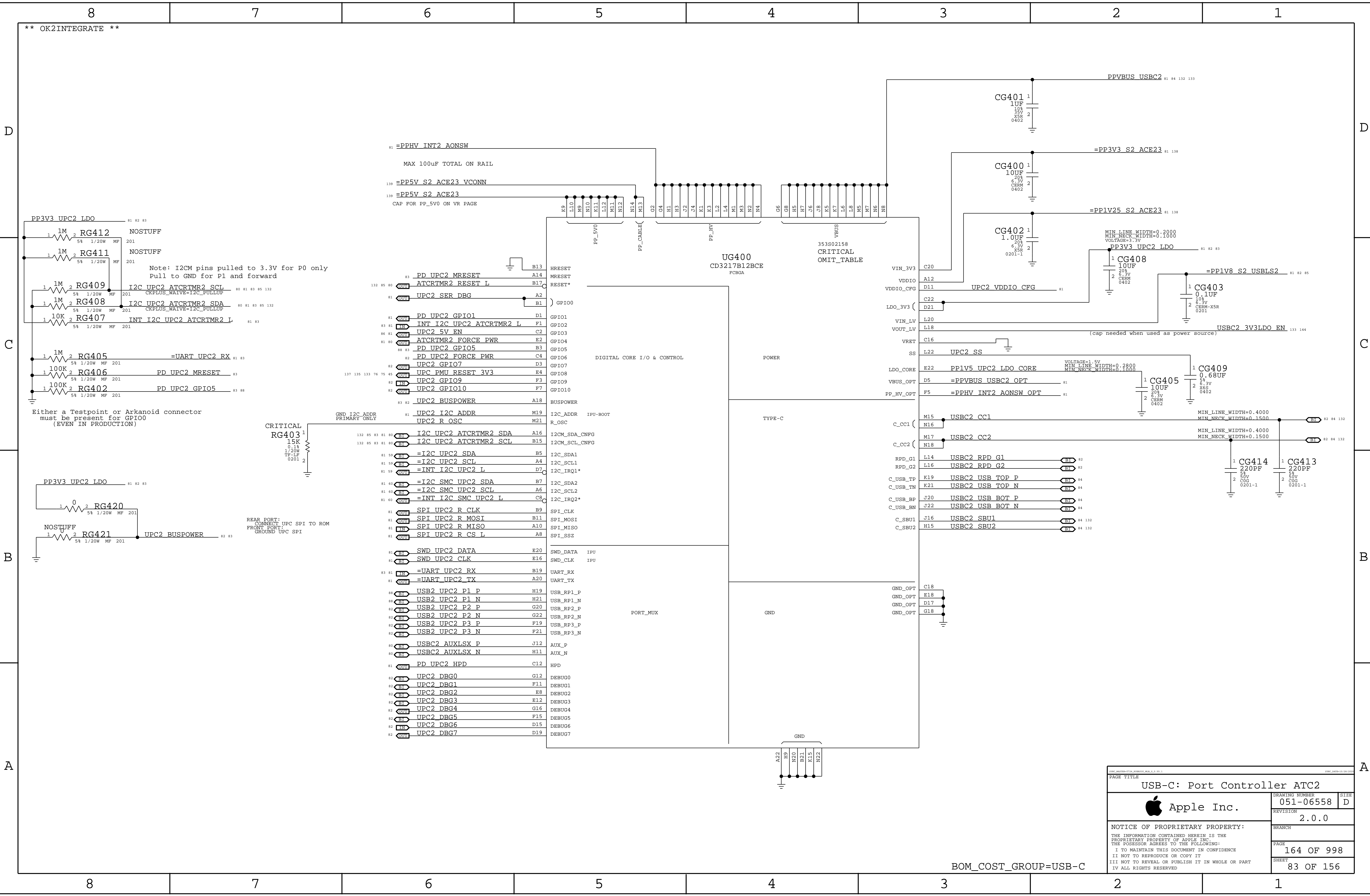
PACK_OPTION=USBC_LAPTOP




Connections for Desktops (No USB-C power in)



BOM_COST_GROUP=USB-C



PAGE TITLE		
USB-C: Port Controller ATC2		
 Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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	PAGE	164 OF 998
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D

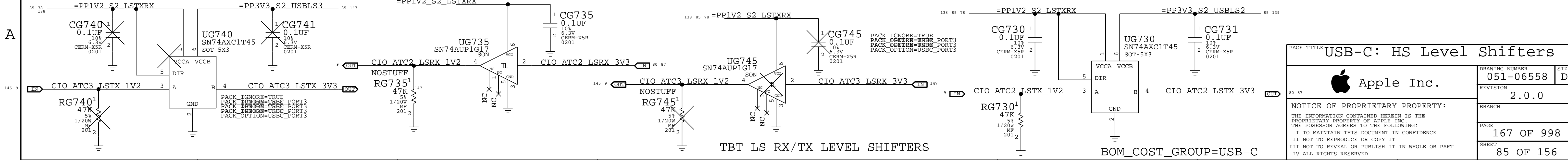
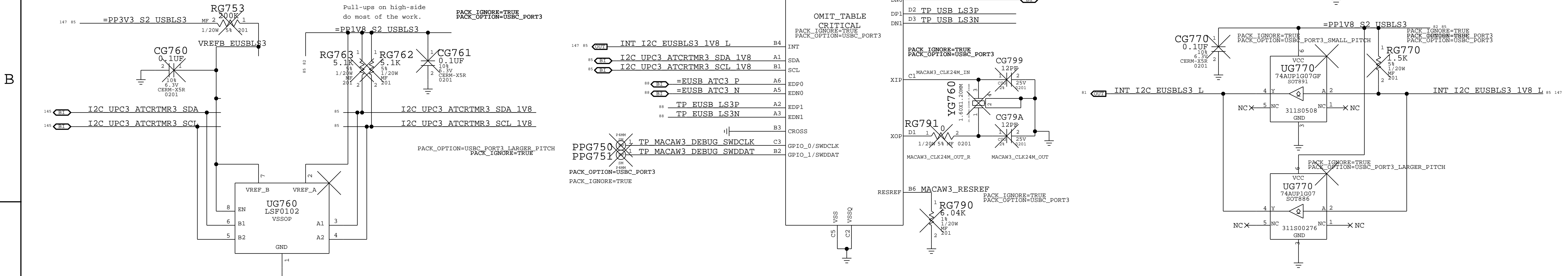


B

A

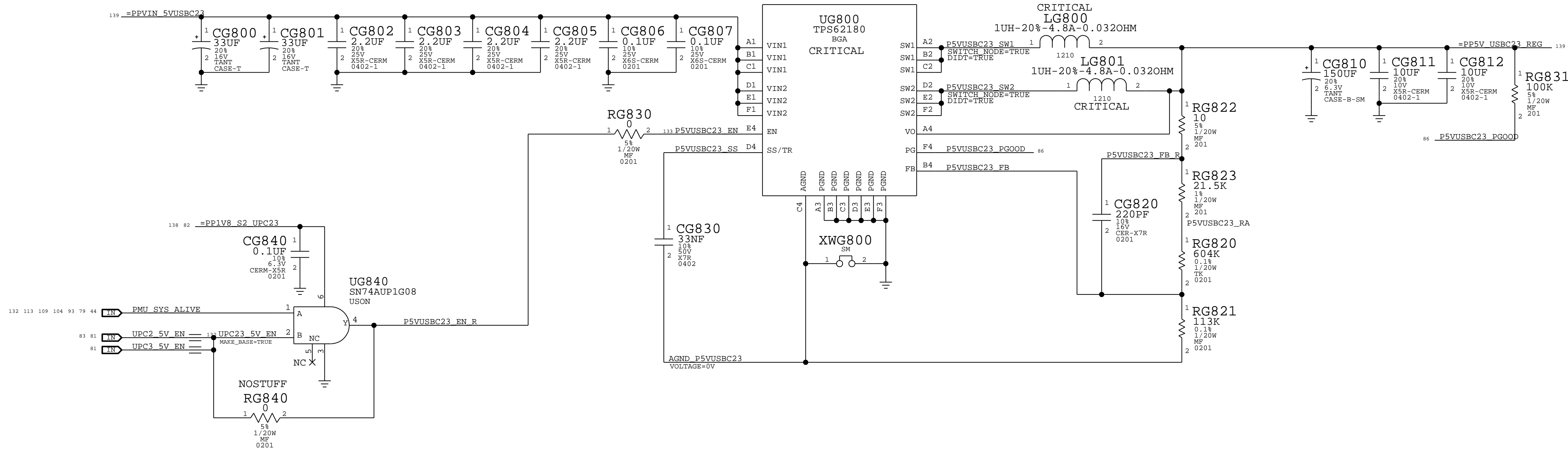


MACAW 2



*** OK2INTEGRATE ***

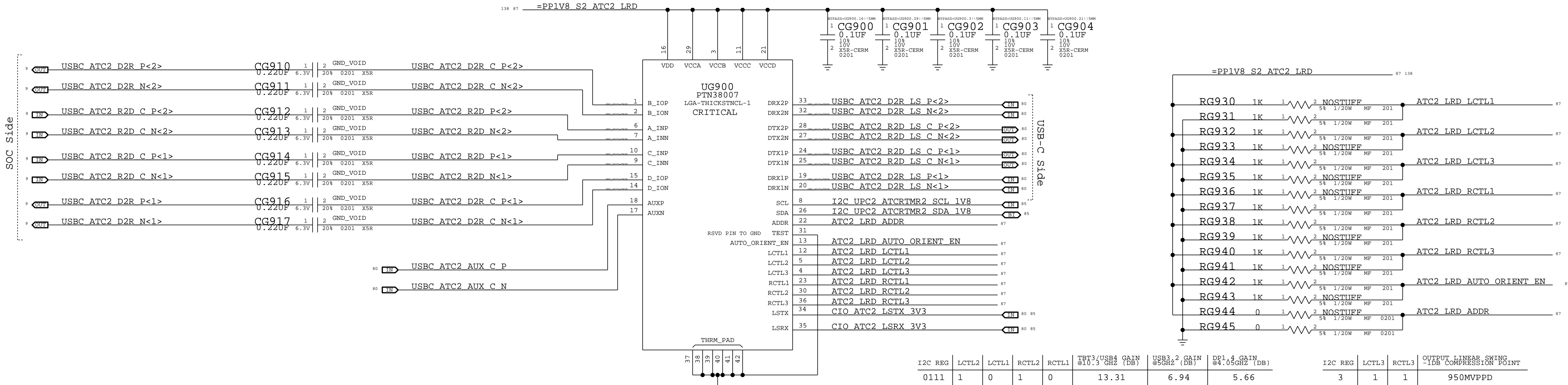
Vout = 5.23V
Freq = 1.9-2.0MHz
OCP Max = 9A
OCP Nom = 7A
OCP Min = 4A
Icc Max = 3.3A



PAGE TITLE		
USB-C: 5V Regulator		
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BOM_COST_GROUP=USB-C

*** In Progress ***



RESISTOR STRAP FOR INITIAL SETTINGS
CAN BE OVERWRITTEN VIA ACE I2C

ATC3 Redriver still in progress
Circuit will be identical to that of ATC2

*** OK2INTEGRATE***

(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)

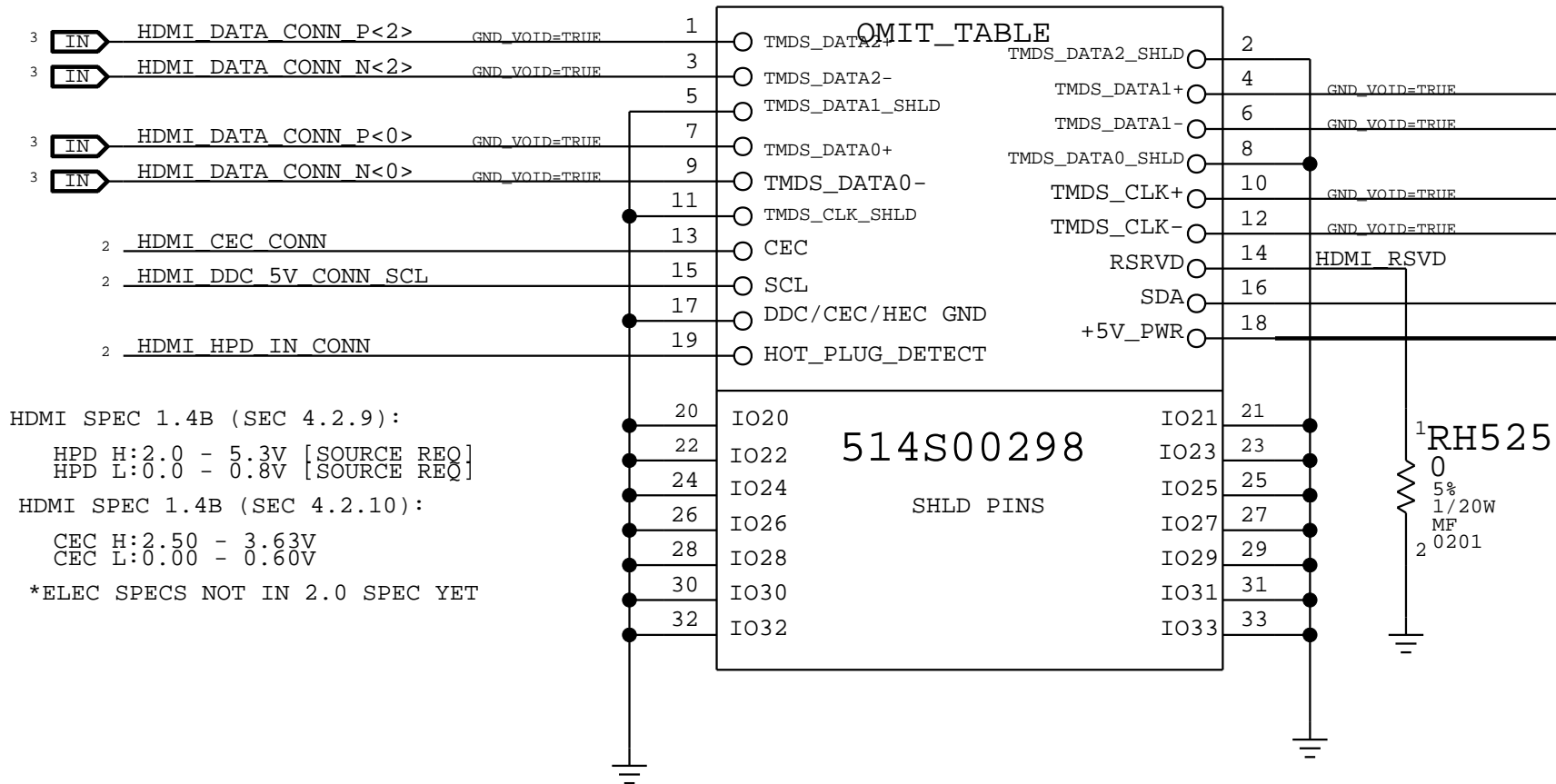
(0.5A OVER-CURRENT LIMIT IMPLEMENTED)

HDMI CONNECTOR THRU-HOLE

JH500
RCPT-HDMI-J314
F-RT-TH

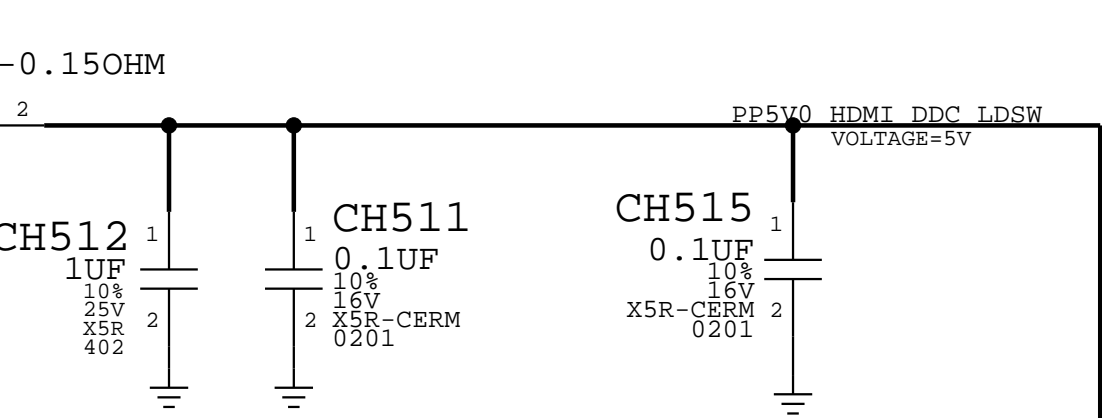
HDMI SPEC 1.4B (SEC 4.2.7):
+5.0V E: 1.8V [SOURCE REQ]
*ELEC SPECS NOT IN 2.0 SPEC YET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0077	377S0183		DZH505	



HDMI SPEC 1.4B (SEC 4.2.9):
HED H:2.0 - 5.3V [SOURCE REQ]
HED L:0.0 - 0.8V [SOURCE REQ]
HDMI SPEC 1.4B (SEC 4.2.10):
CEC H:2.50 - 3.63V
CEC L:0.00 - 0.60V
*ELEC SPECS NOT IN 2.0 SPEC YET

CAPACITANCE = 0.4PF
CLAMPING VOLTAGE = 7.0V
IEC 61000-4-2 ESD: 1(-30KV (AIR), +/-25KV (CONTACT))
IEC 61000-4-4 EFT: 40A (5V50NS)
IEC 61000-4-5 SURGE: 5A (8/20US)

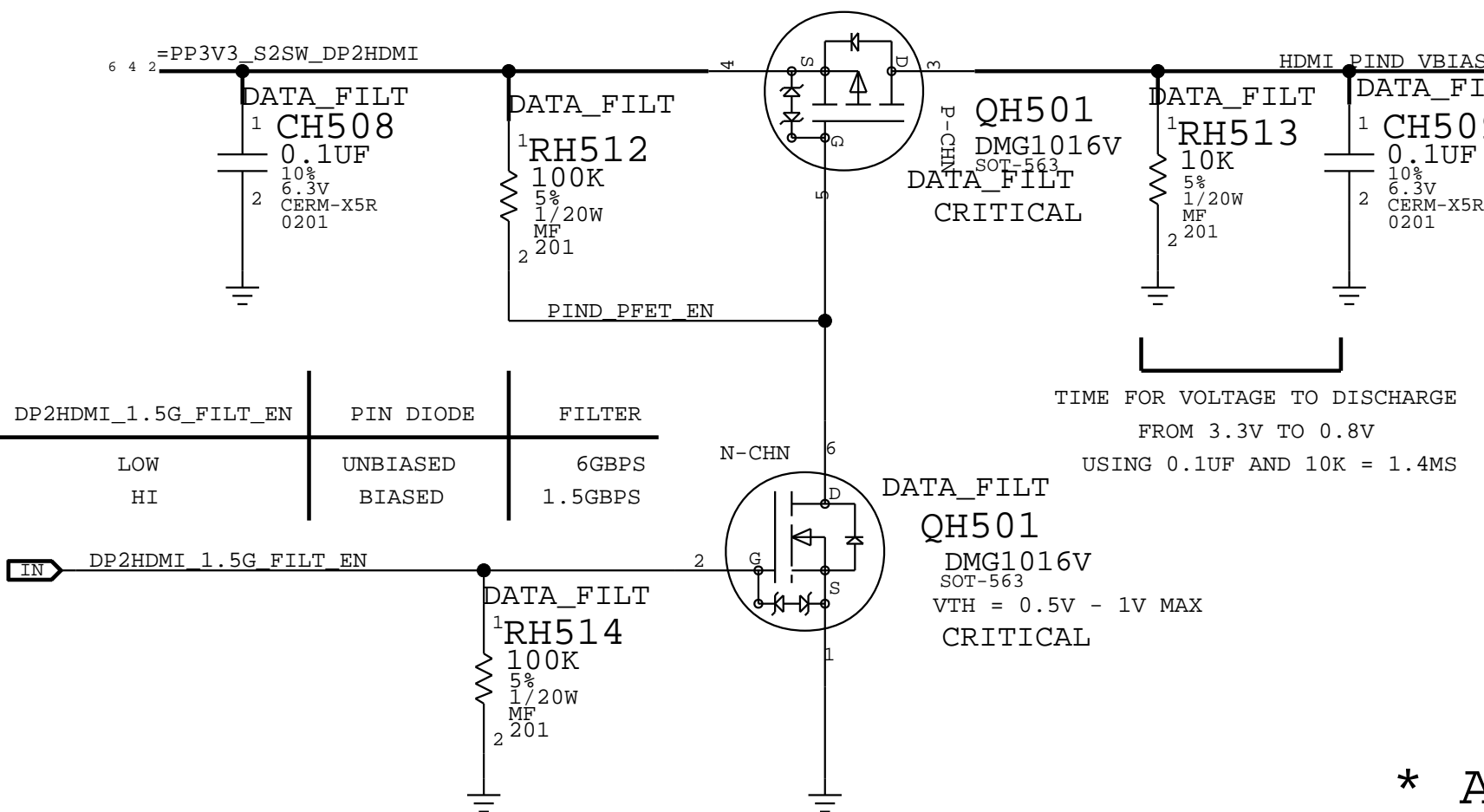
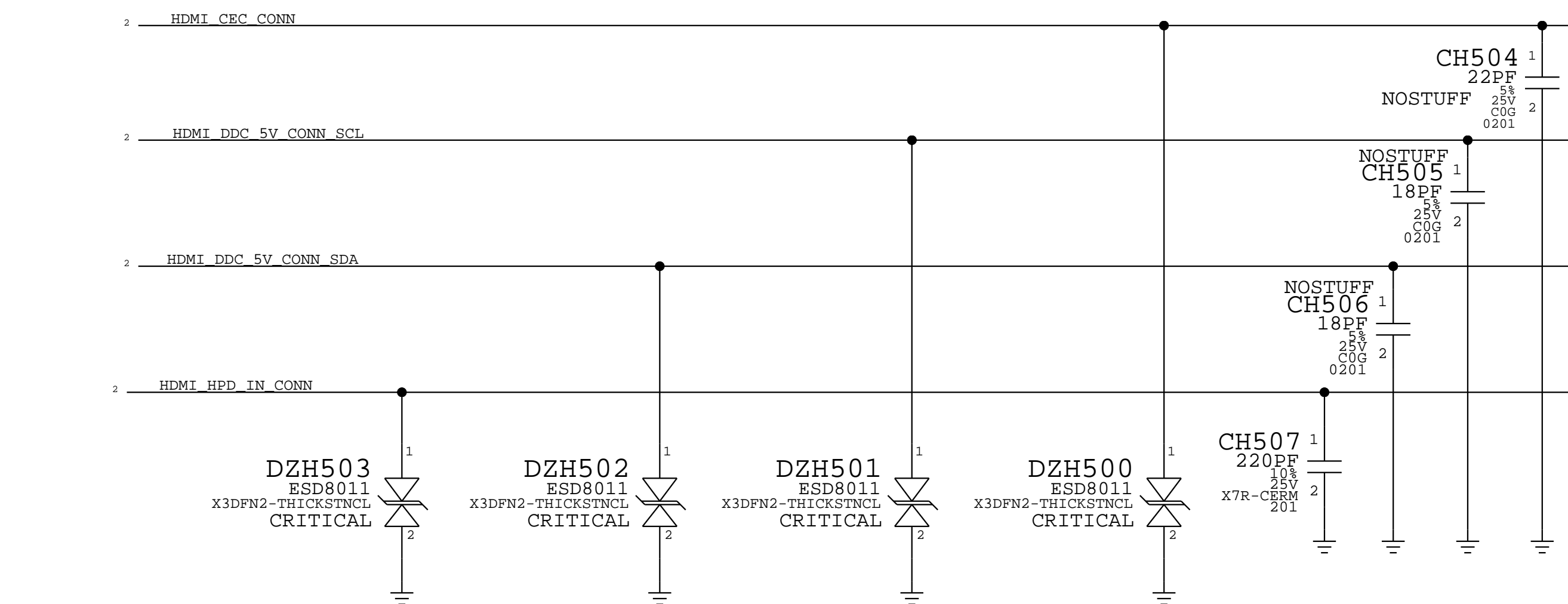


CRITICAL
LH504
FERR-470-OHM-215MA-1.5OHM

CRITICAL
LH501
FERR-470-OHM-215MA-1.5OHM

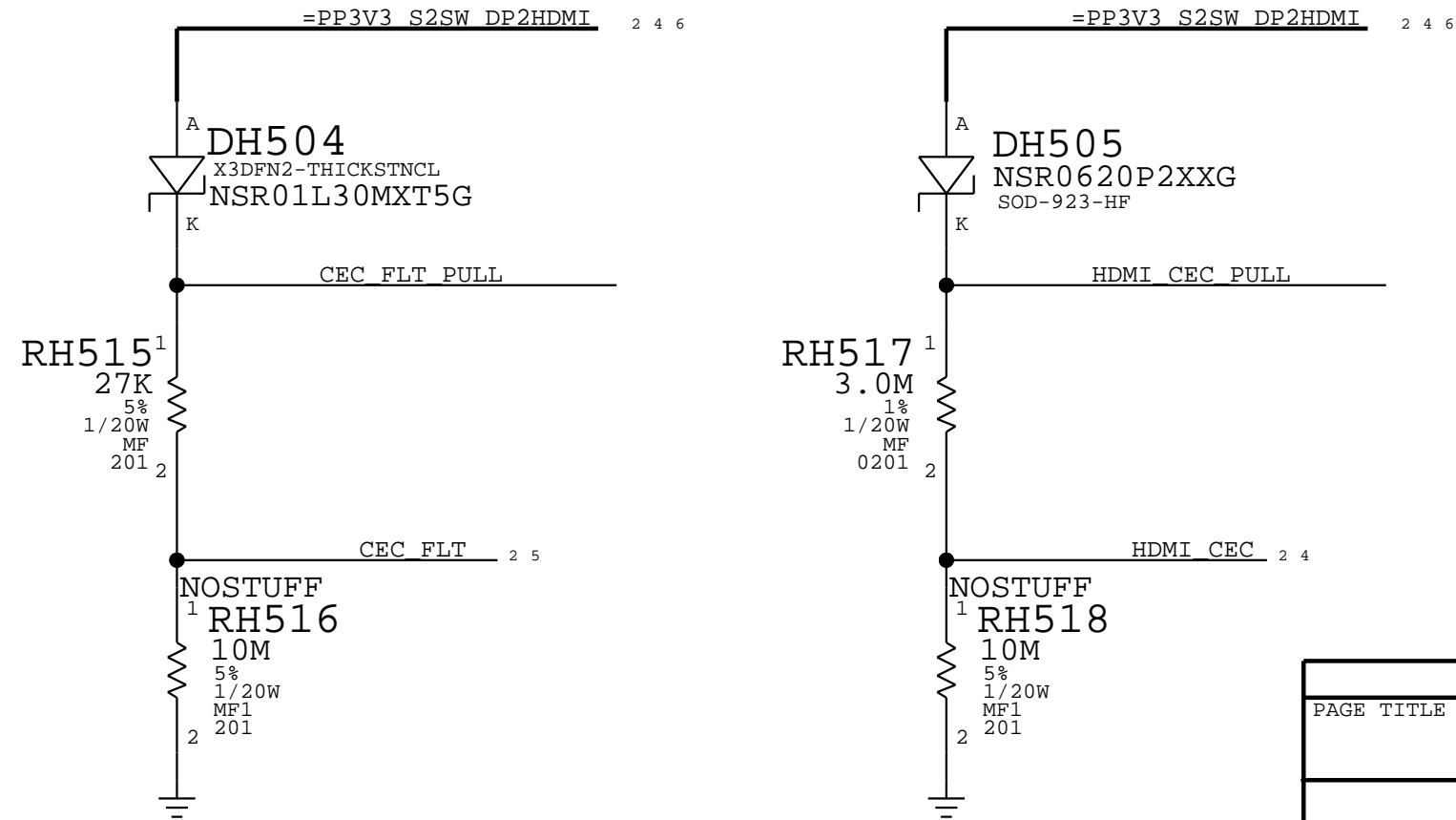
CRITICAL
LH502
FERR-470-OHM-215MA-1.5OHM

CRITICAL
LH503
FERR-470-OHM-215MA-1.5OHM



PIN DIODE VOLTAGE DROP = 0.8V
CURRENT PER DIODE:
(3.3V - 0.8V) / 1K = 2.5MA
CURRENT THROUGH 16 DIODES = 40MA

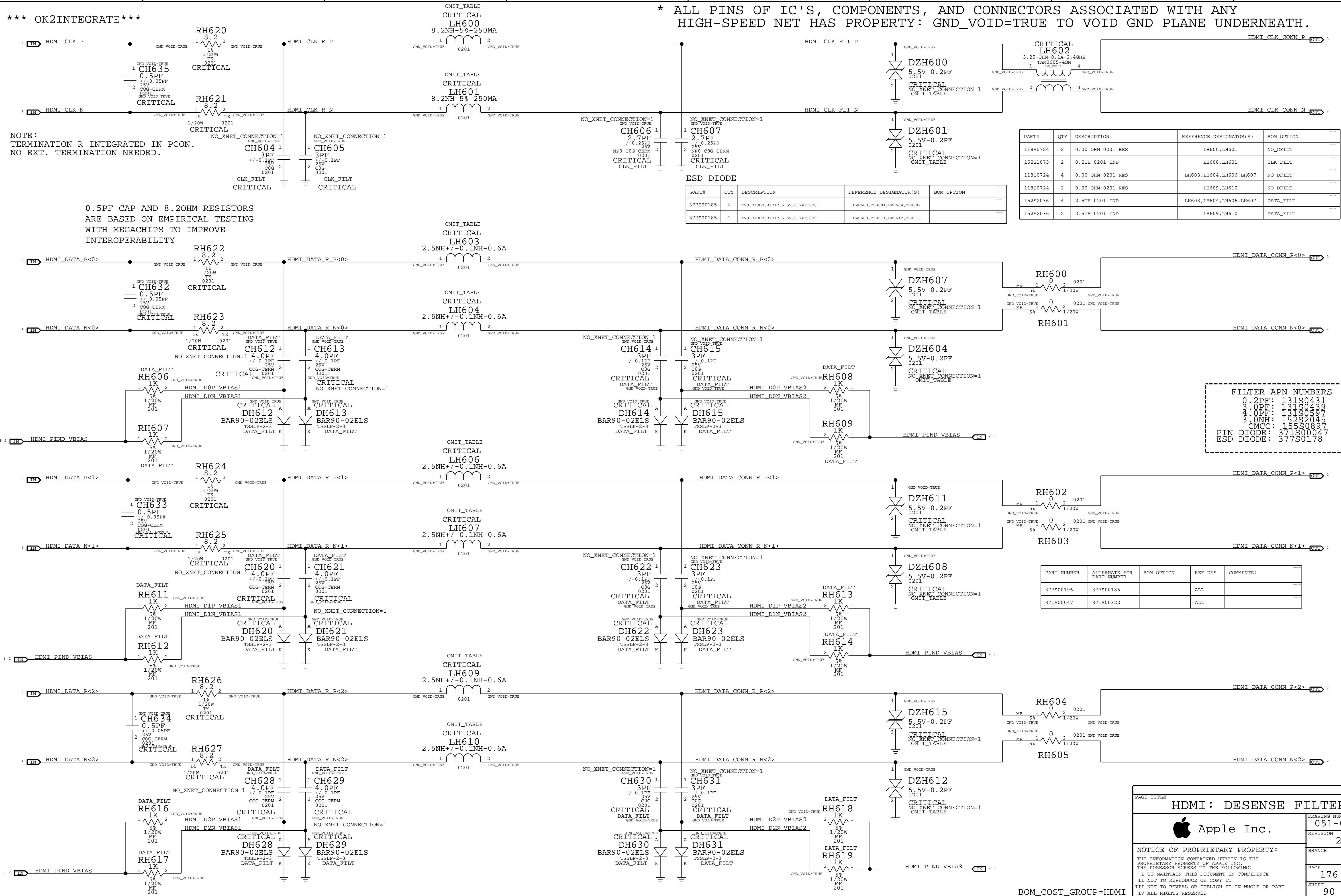
TIME FOR VOLTAGE TO DISCHARGE
FROM 3.3V TO 0.8V
USING 0.1UF AND 10K = 1.4MS

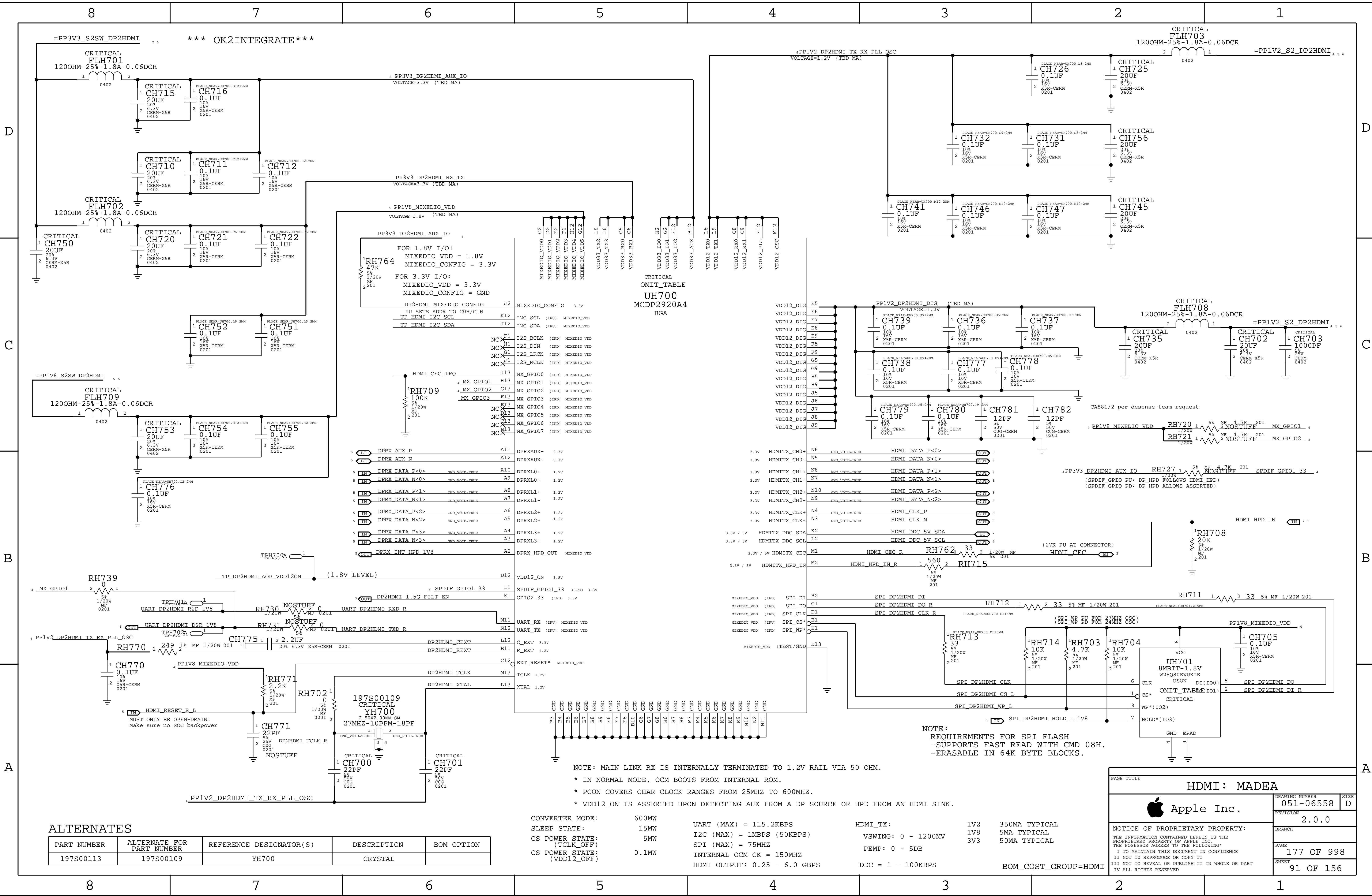


PAGE TITLE		
HDMI : CONNECTOR		
	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY
HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

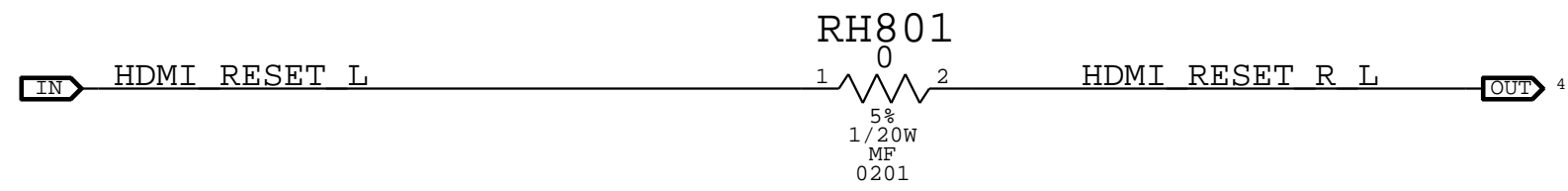
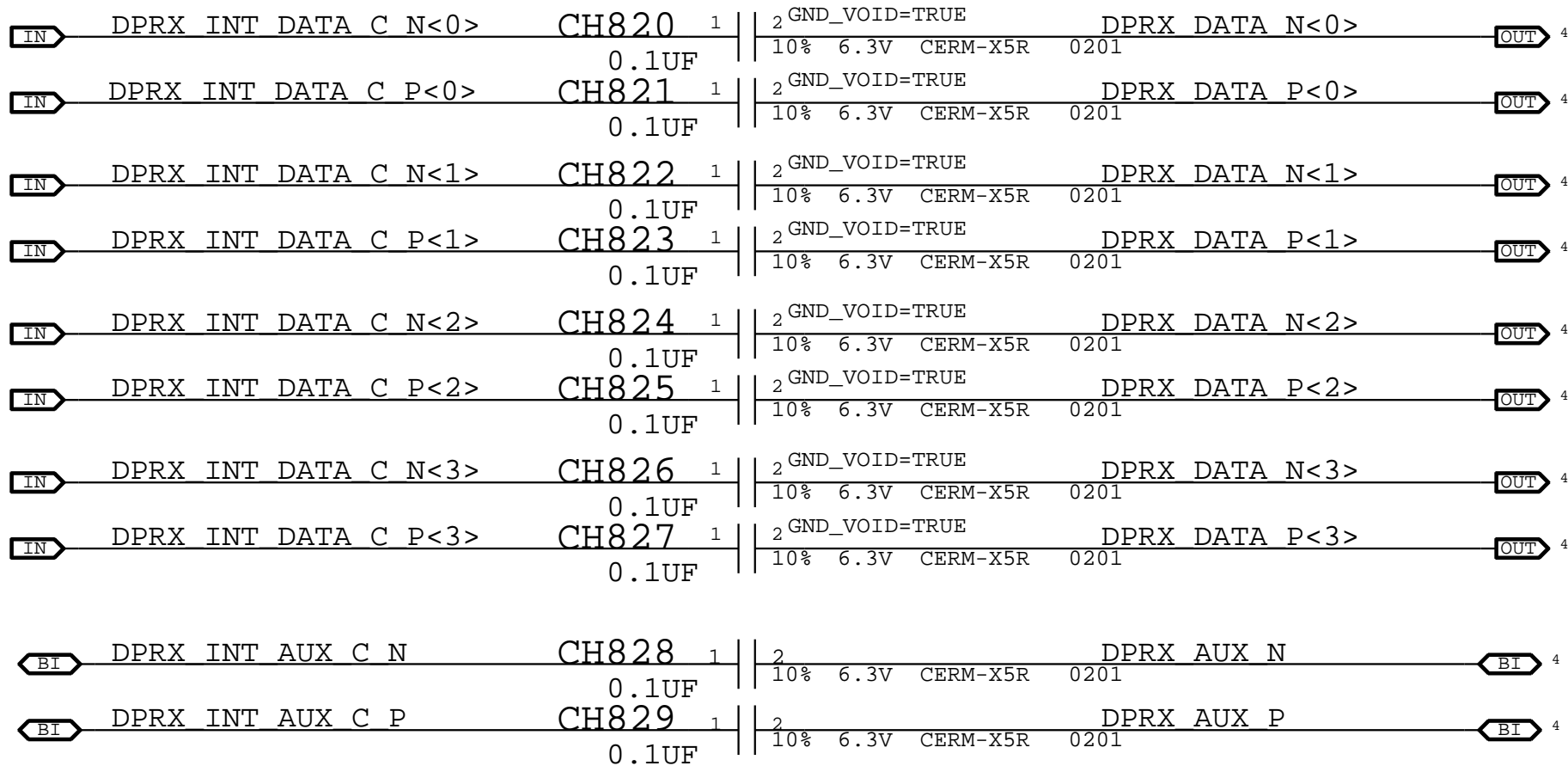
BOM_COST_GROUP=HDMI





*** OK2INTEGRATE***

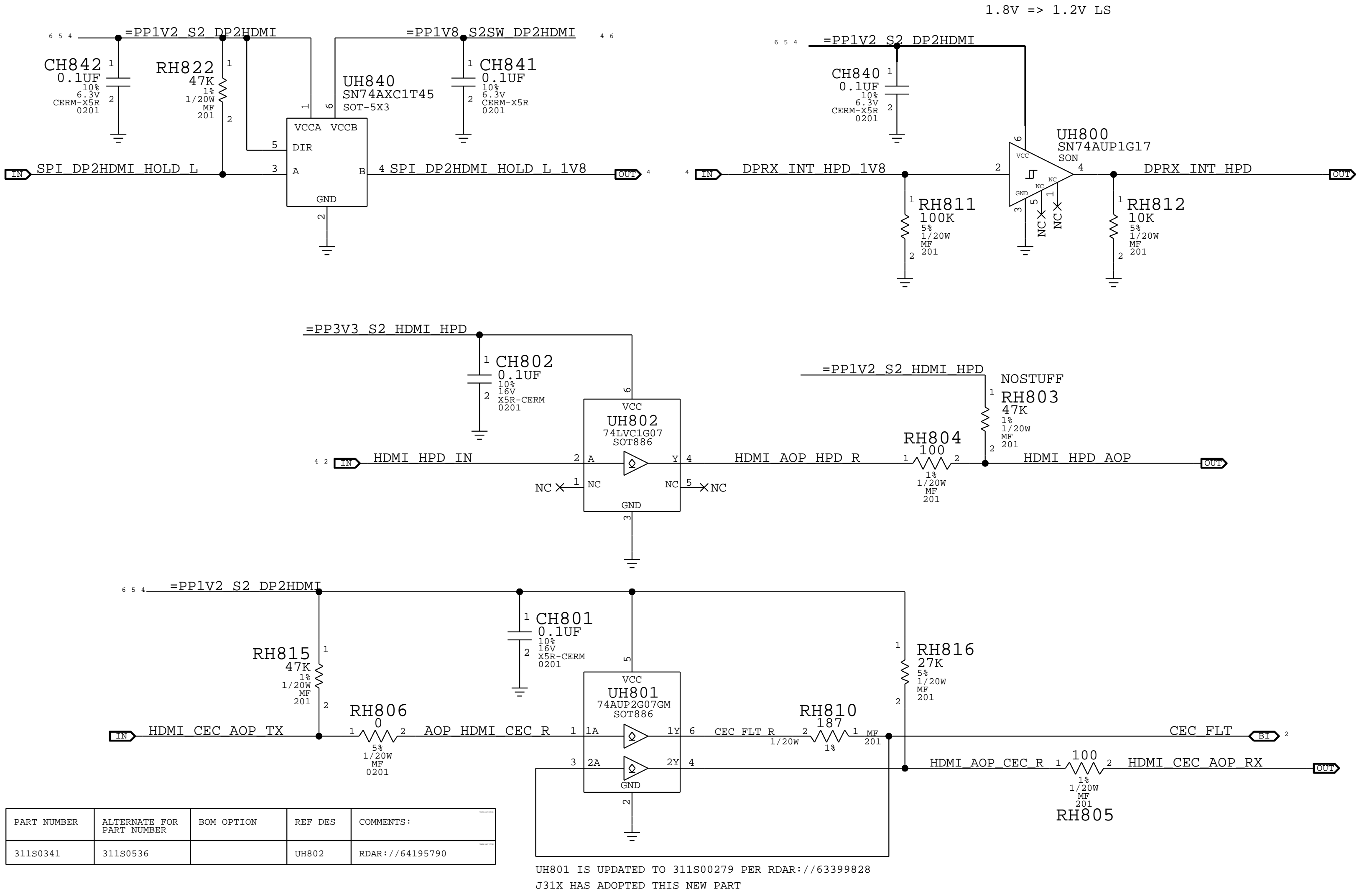
LPDP AC Caps



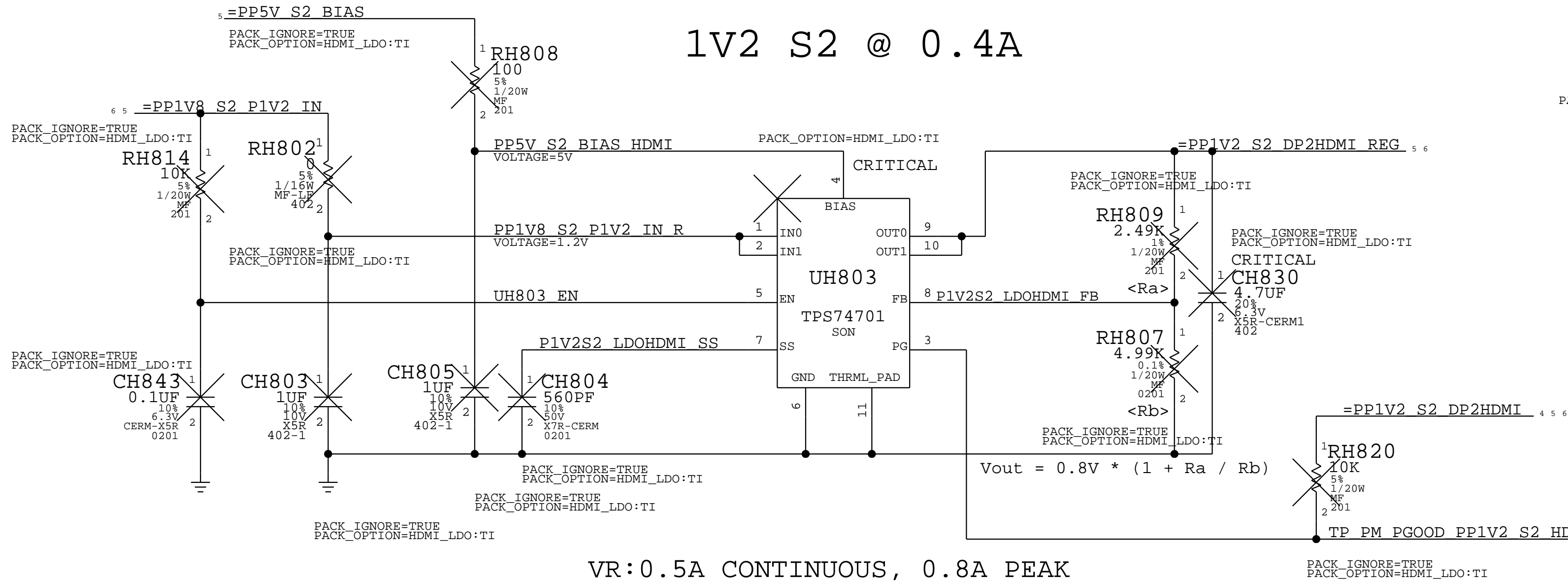
HDMI ROM BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S00049	1	MADBA SPI FLASH, 8MB, 1.8V, 8P, USON	UH701	HDMI_ROM:BLANK
341S01592	1	IC, HDMI ROM, FW V1.130, X1814	UH701	HDMI_ROM:FW_V1P130
341S01701	1	ROM, HDMI (VXXX), PROTO=0, X2737	UH701	HDMI_ROM:PROTO0

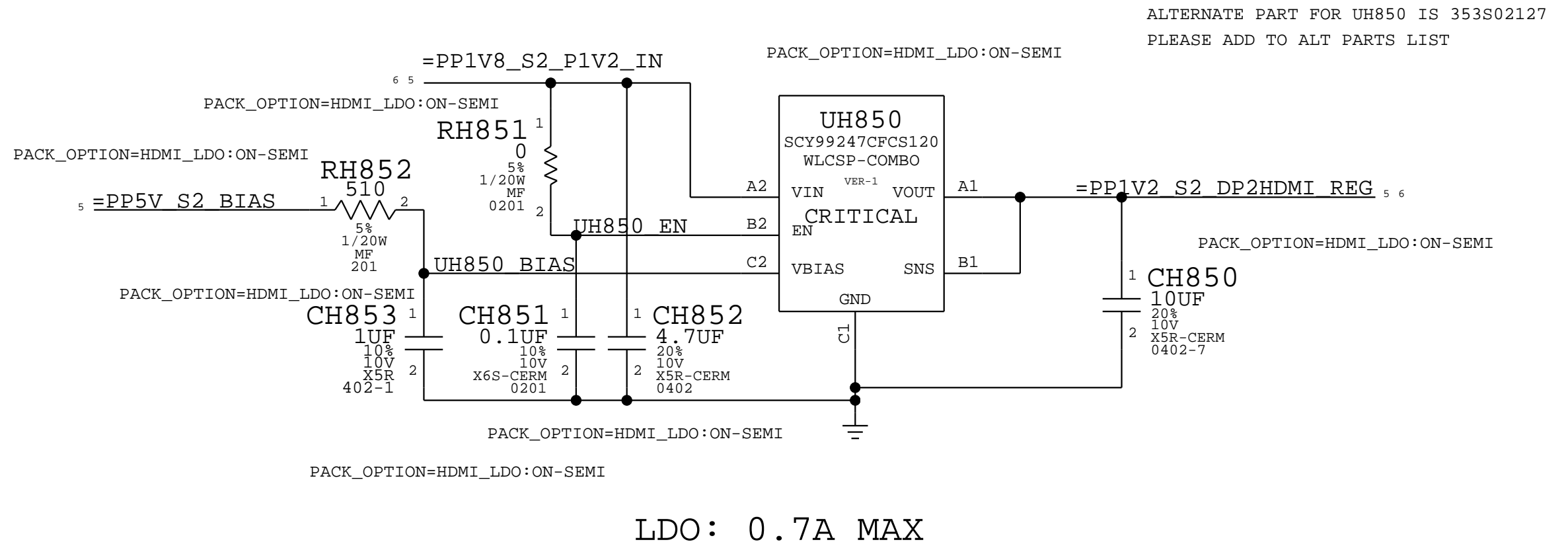
LEVEL SHIFTERS



HDMI 1V2 VR



1V2 S2 @ 350MA LOAD



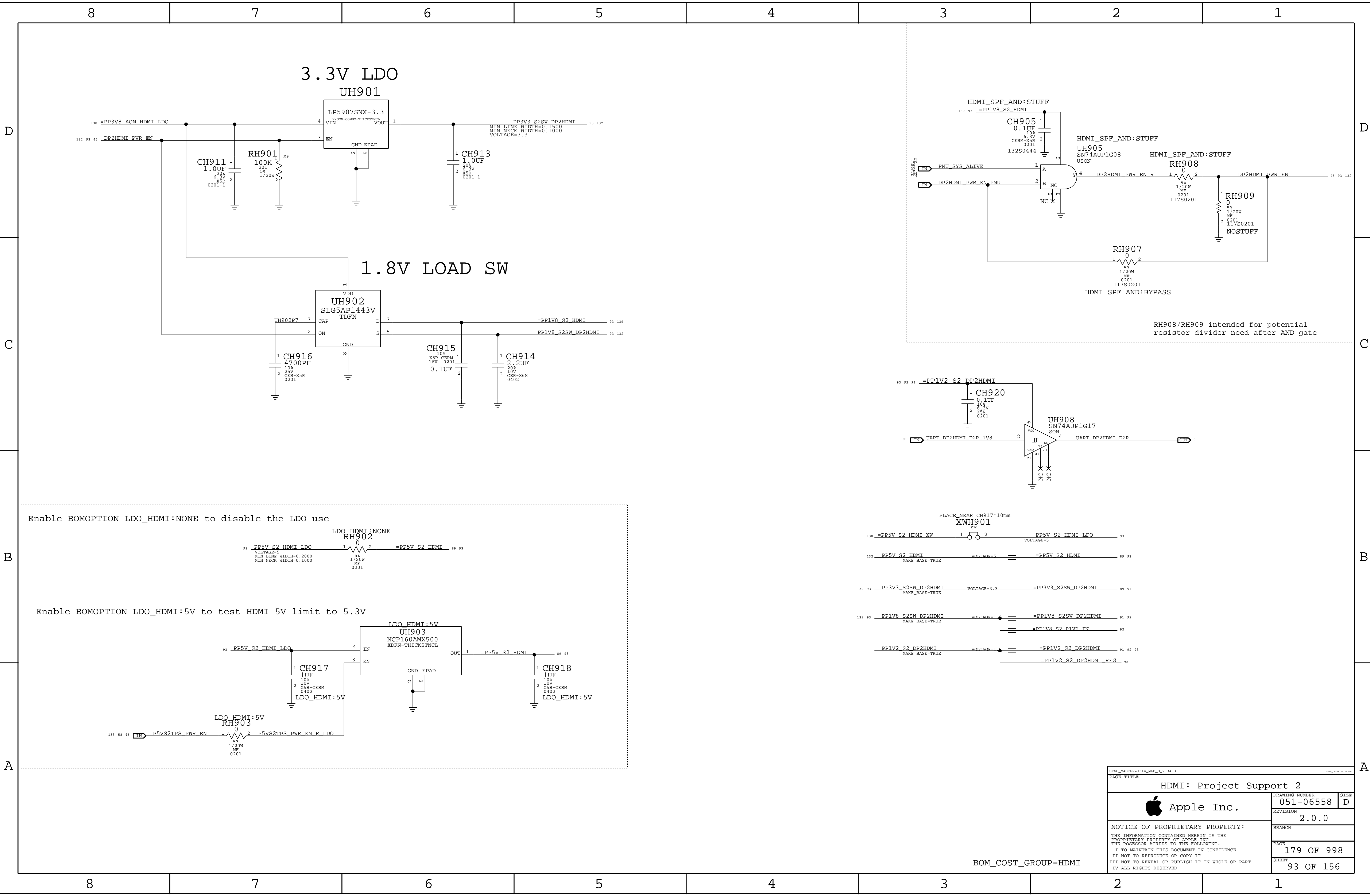
LDO: 0.7A MAX

VR:0.5A CONTINUOUS, 0.8A PEAK

THE LDO IS A CHEAPER PART COMPARED TO TI PART

BOM_COST_GROUP=HDMI

PAGE TITLE		
HDMI: Project Support 1		
Apple Inc.	DRAWING NUMBER	051-06558
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3.3V LDO

UH901

1.8V LOAD SW

UH902

SLG5AP1443V

TDFN

GND

UH902E7

ON

CAP

VDD

1

2

3

4

5

6

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9

10

11

12

13

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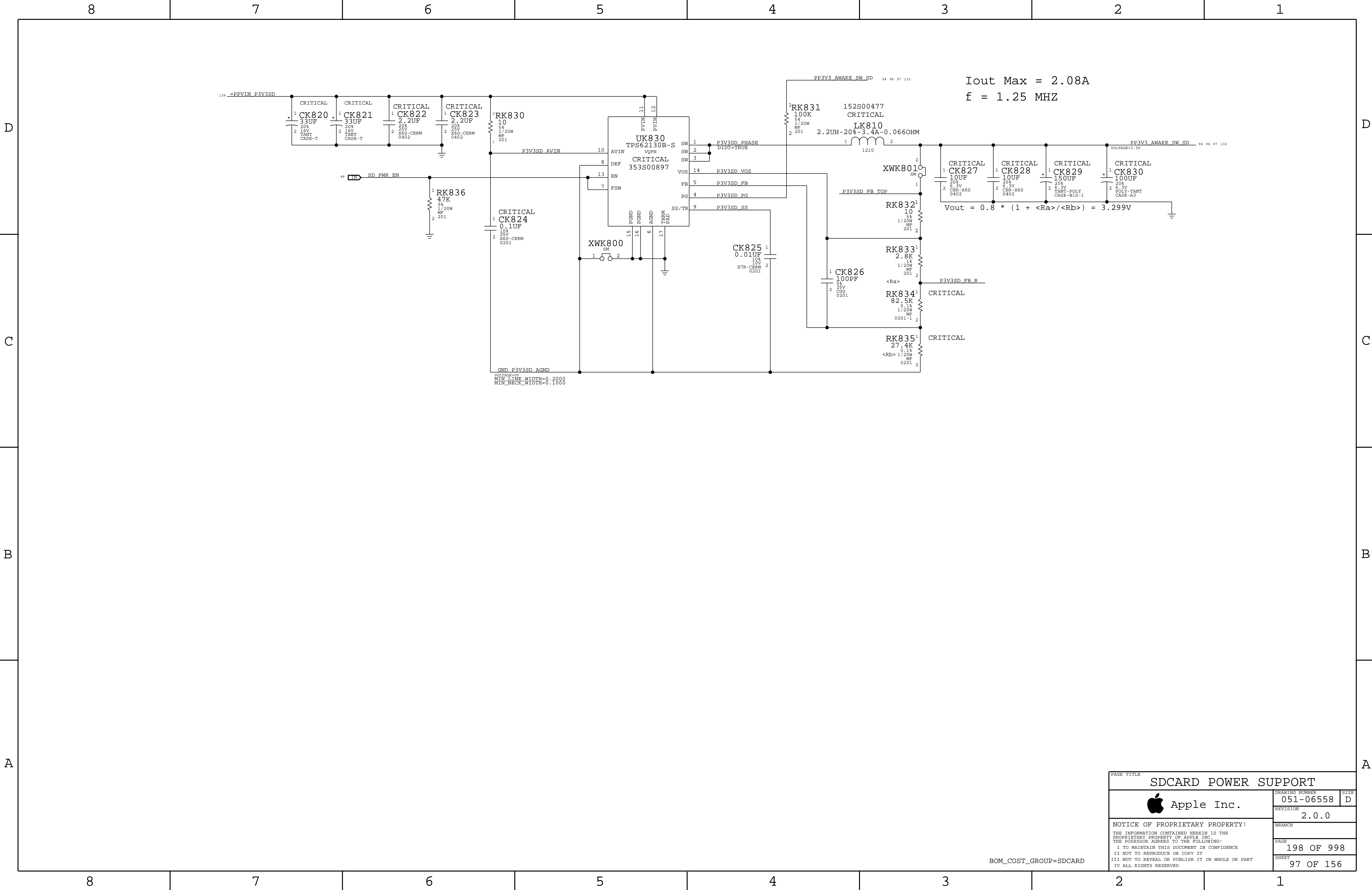
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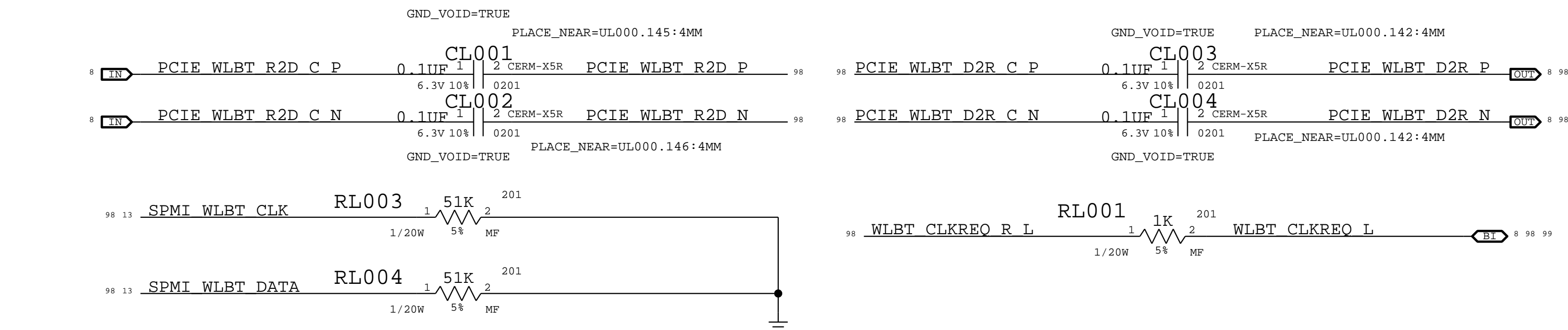
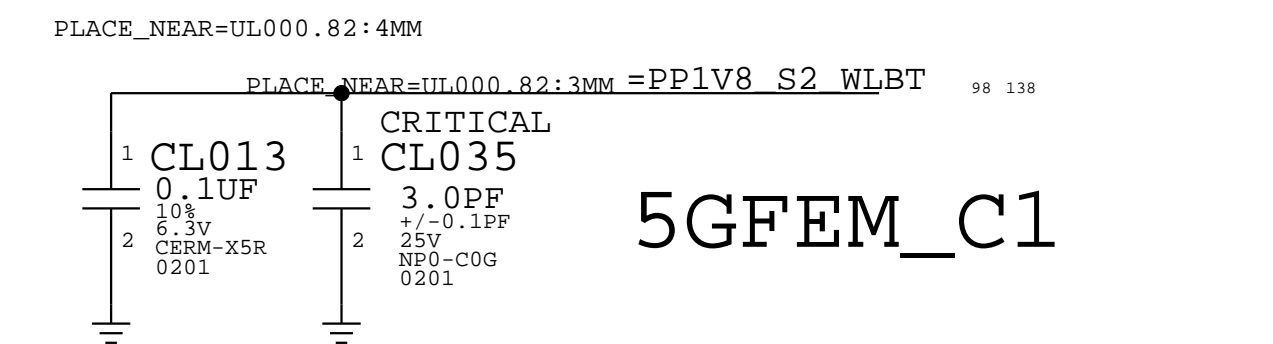




PAGE TITLE		
SDCARD POWER SUPPORT		
 Apple Inc.	DRAWING NUMBER	051-06558
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BOM_COST_GROUP=SDCARD

FOR SYSTEM INTEGRATION INFORMATION REFER TO
RDAR://PROBLEM/59047597



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00858	339S00813	ANY	UL000	TYPHOON ES2.7
339S00859	339S00813	ANY	UL000	TYPHOON ES2.9

PPL026	P2MM SM	PLACE_NEAR=U0600.A41:10MM	
	(P)	PCIE WLBT D2R P	8 98
	PLACE_SIDE=BOTTOM		
PPL027	P2MM SM	PLACE_NEAR=U0600.B41:10MM	
	(P)	PCIE WLBT D2R N	8 98
	PLACE_SIDE=BOTTOM		

PAGE TITLE			
WIFI/BT: MODULE			
 Apple Inc.	DRAWING NUMBER		SIZE
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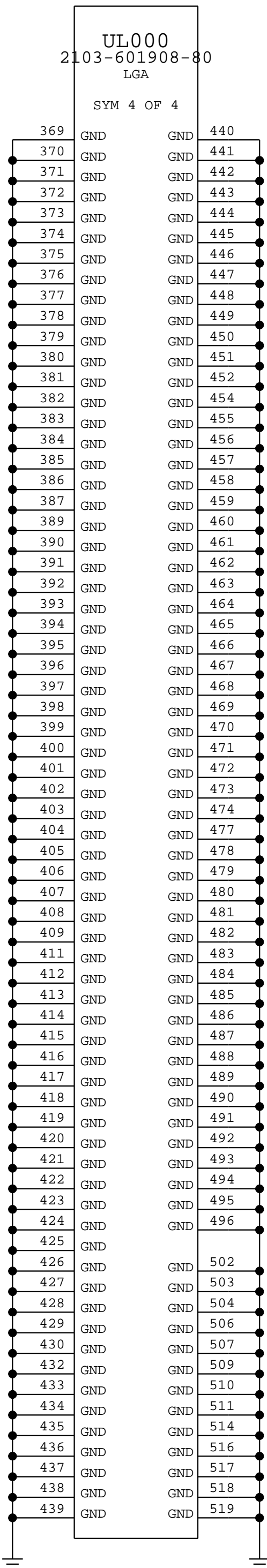
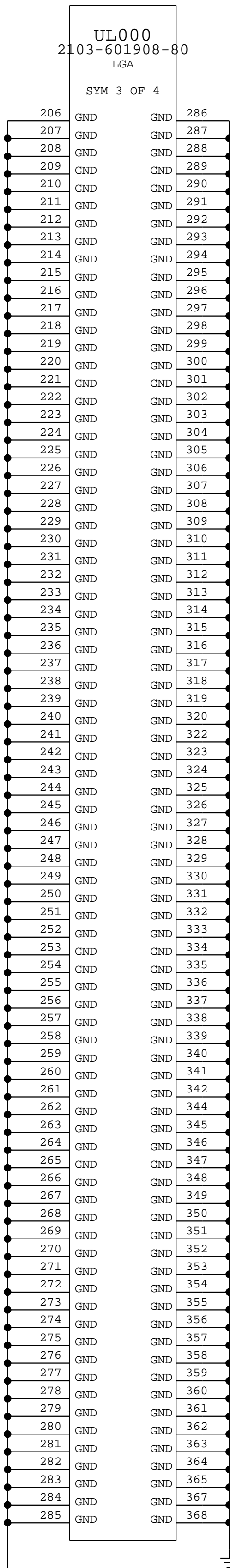
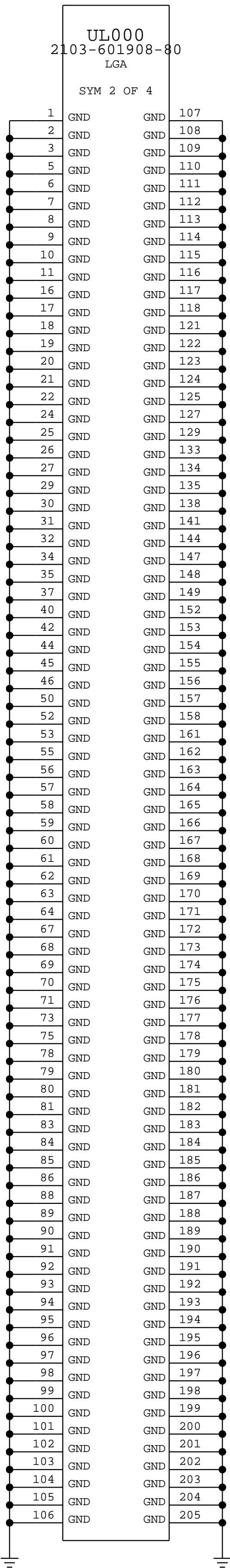
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8 7 6 5 4 3 2 1

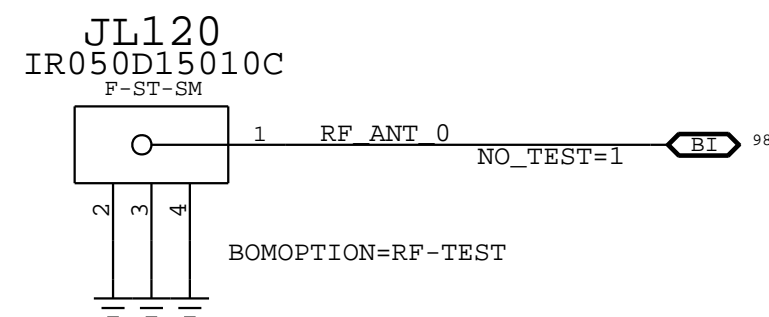
*** IN PROGRESS ***

TYPHOON WIFI/BT MODULE GND

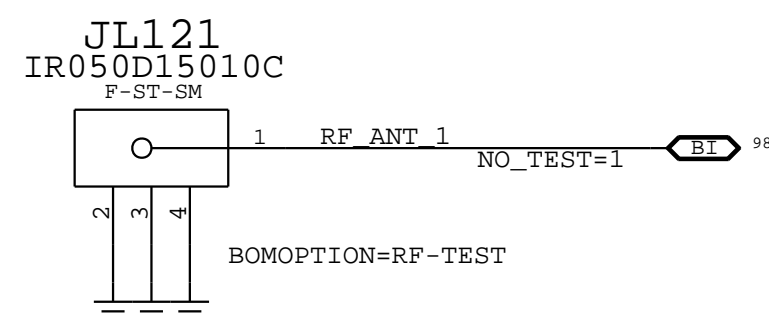
ANTENNA CONNECTORS



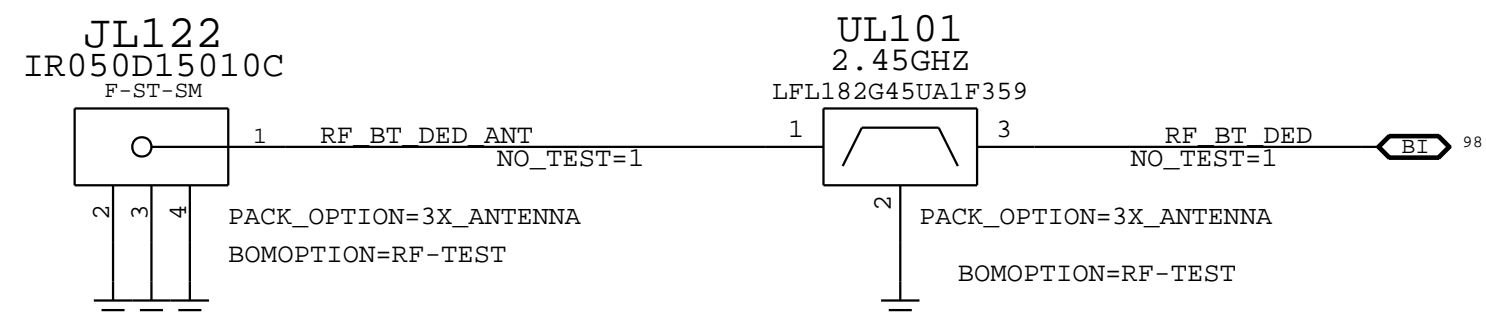
2G_C0
5G_C0
BT_C0



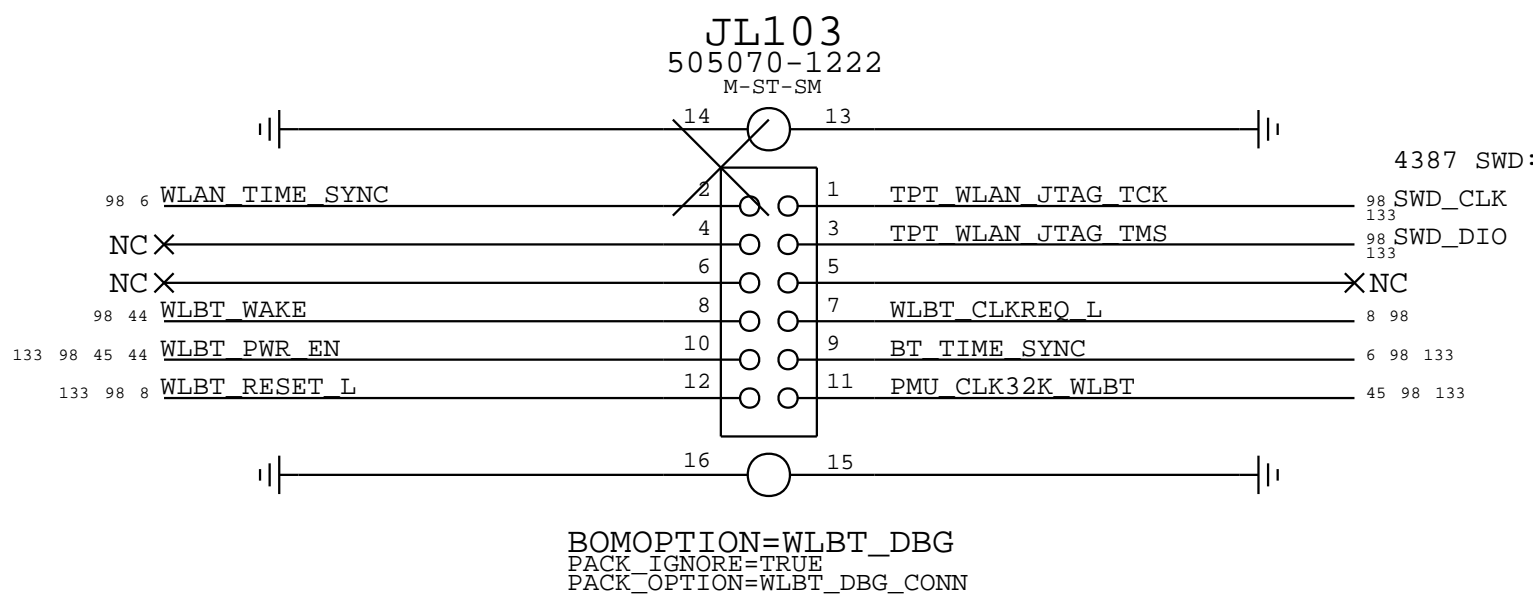
2G_C1
5G_C1
BT_C1



BT_C1_DED



WLBT DEBUG CONNECTOR

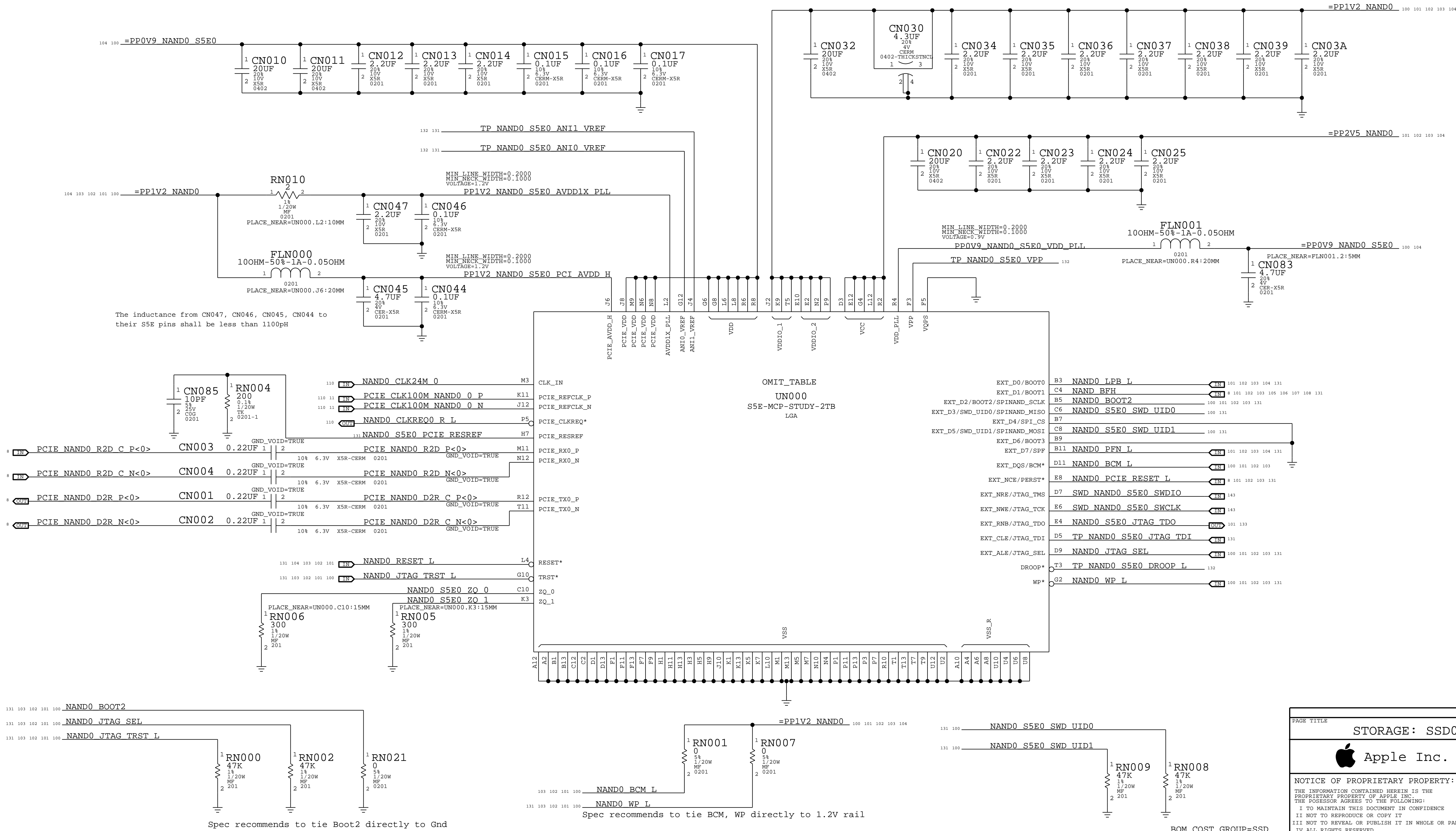


BOM_COST_GROUP=WIRELESS

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WIFI/BT: ANTENNA and GND		
	DRAWING NUMBER	051-06558
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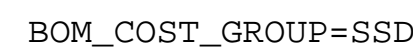
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NAND0 S5E0



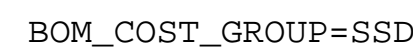
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NAND0 S5E1



PAGE TITLE			
STORAGE: SSD0 S5E <1>			
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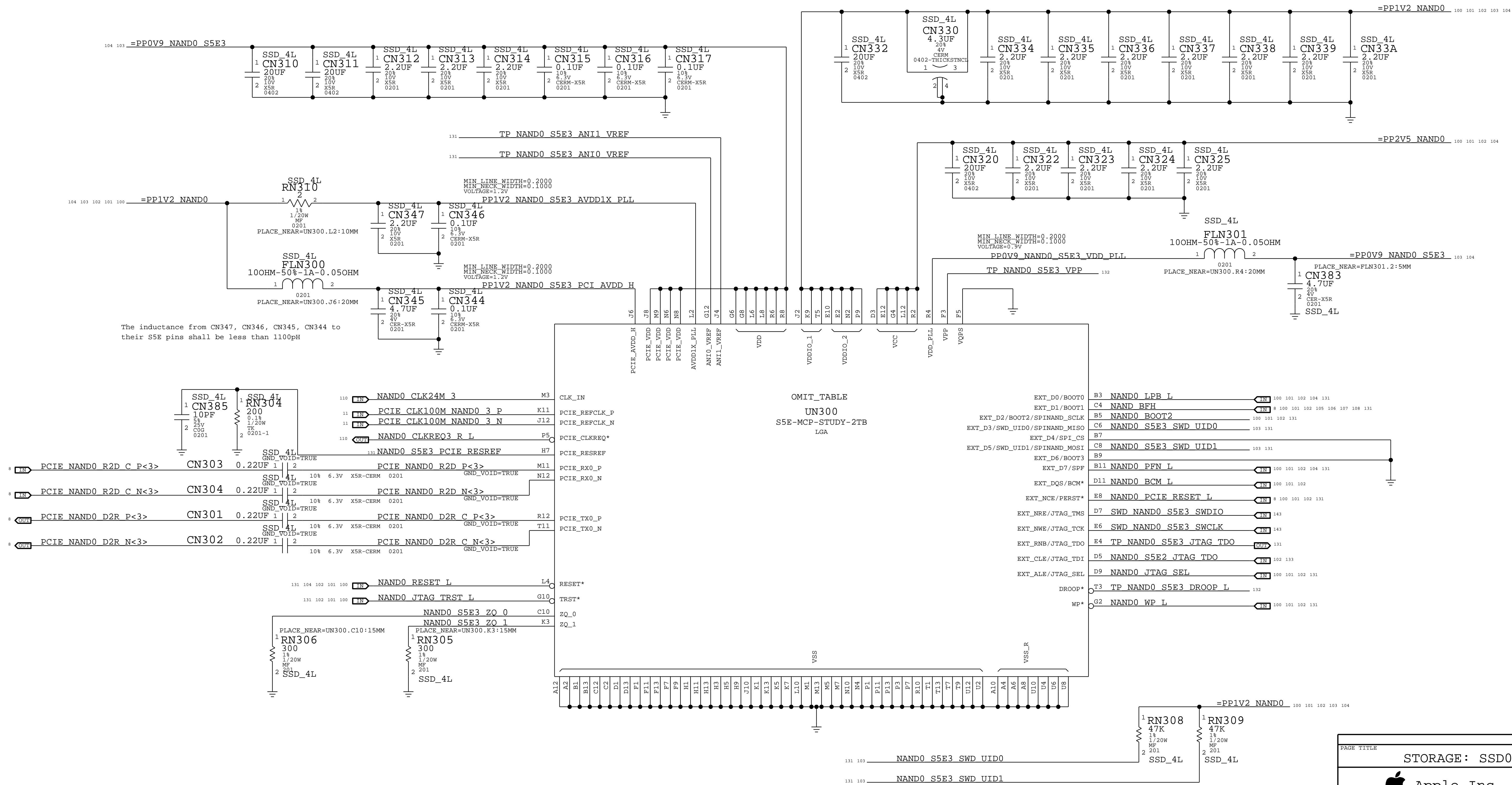
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BRANCH		
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*** OK2INTEGRATE ***

NAND0	S5E3
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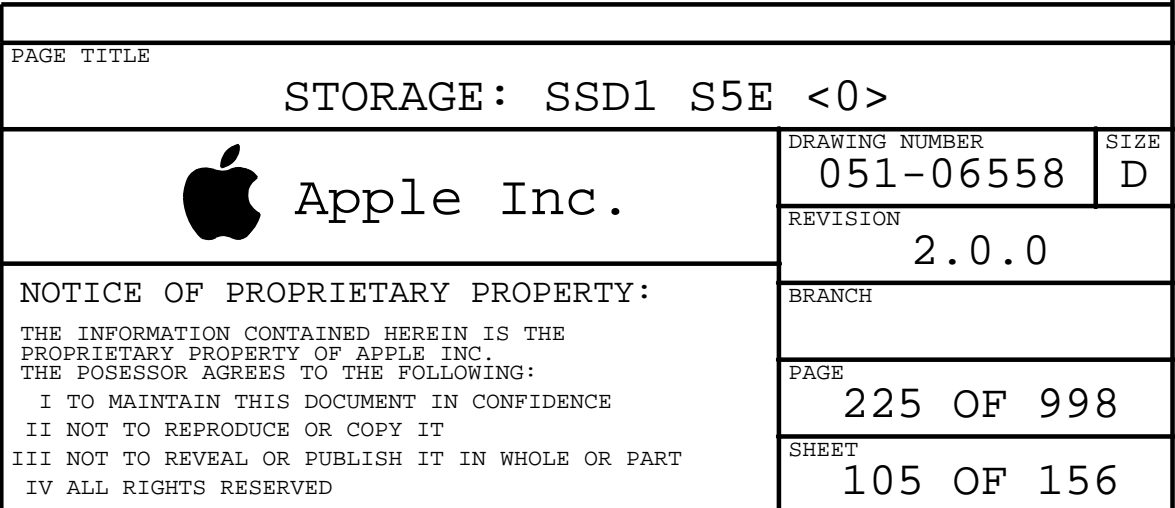


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STORAGE: SSD0 S5E <3>		
 Apple Inc.	DRAWING NUMBER	SIZE
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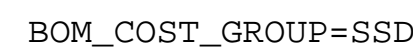
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NAND1 S5E0



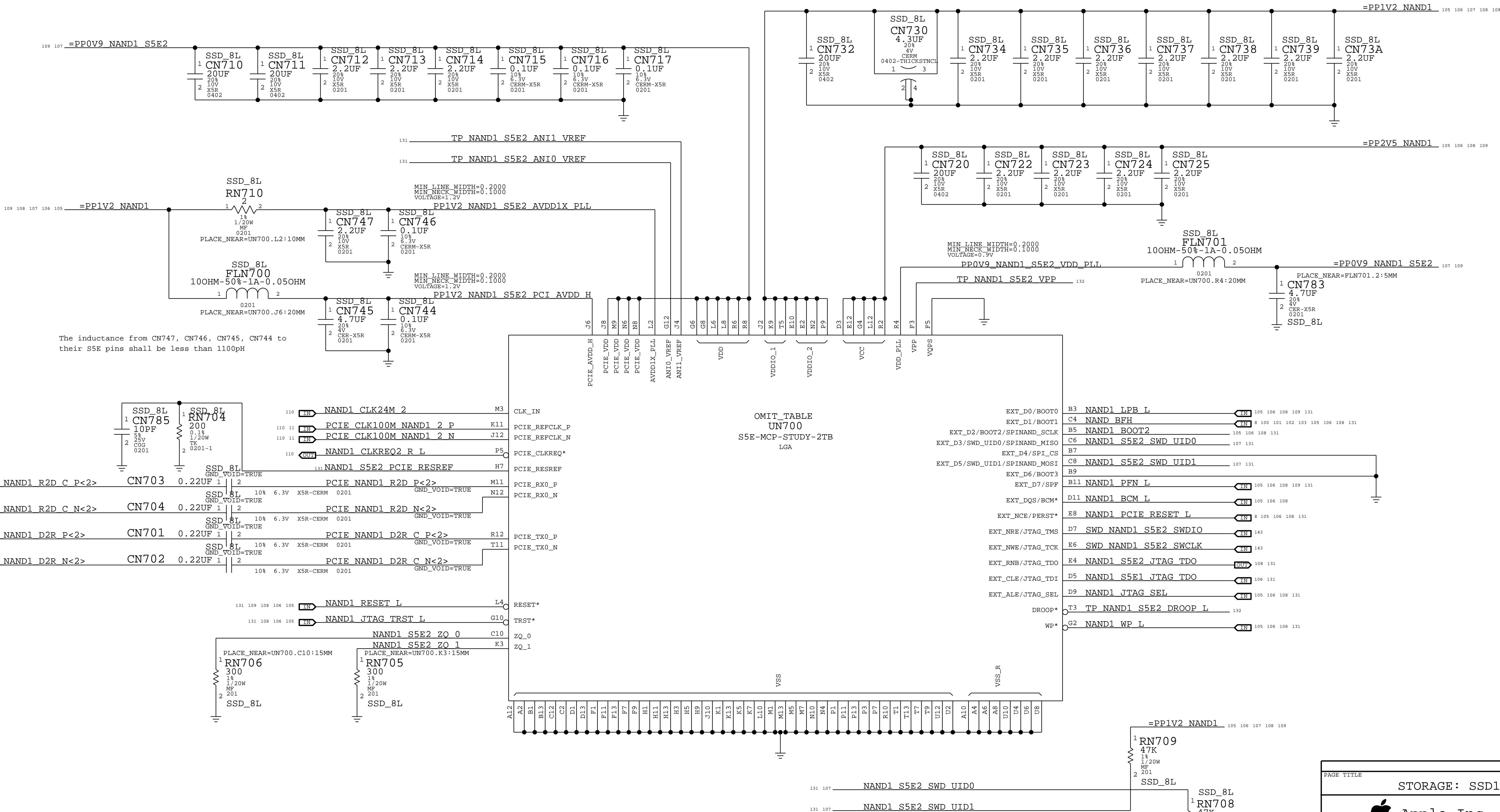
NAND1 S5E1



PAGE TITLE			
STORAGE: SSD1 S5E <1>			
 Apple Inc.	DRAWING NUMBER		SIZE
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*** OK2INTEGRTE ***

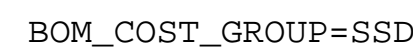
NAND1 S5E2




PAGE TITLE			
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	REVISION	2.0.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
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I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	107 OF 156
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III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

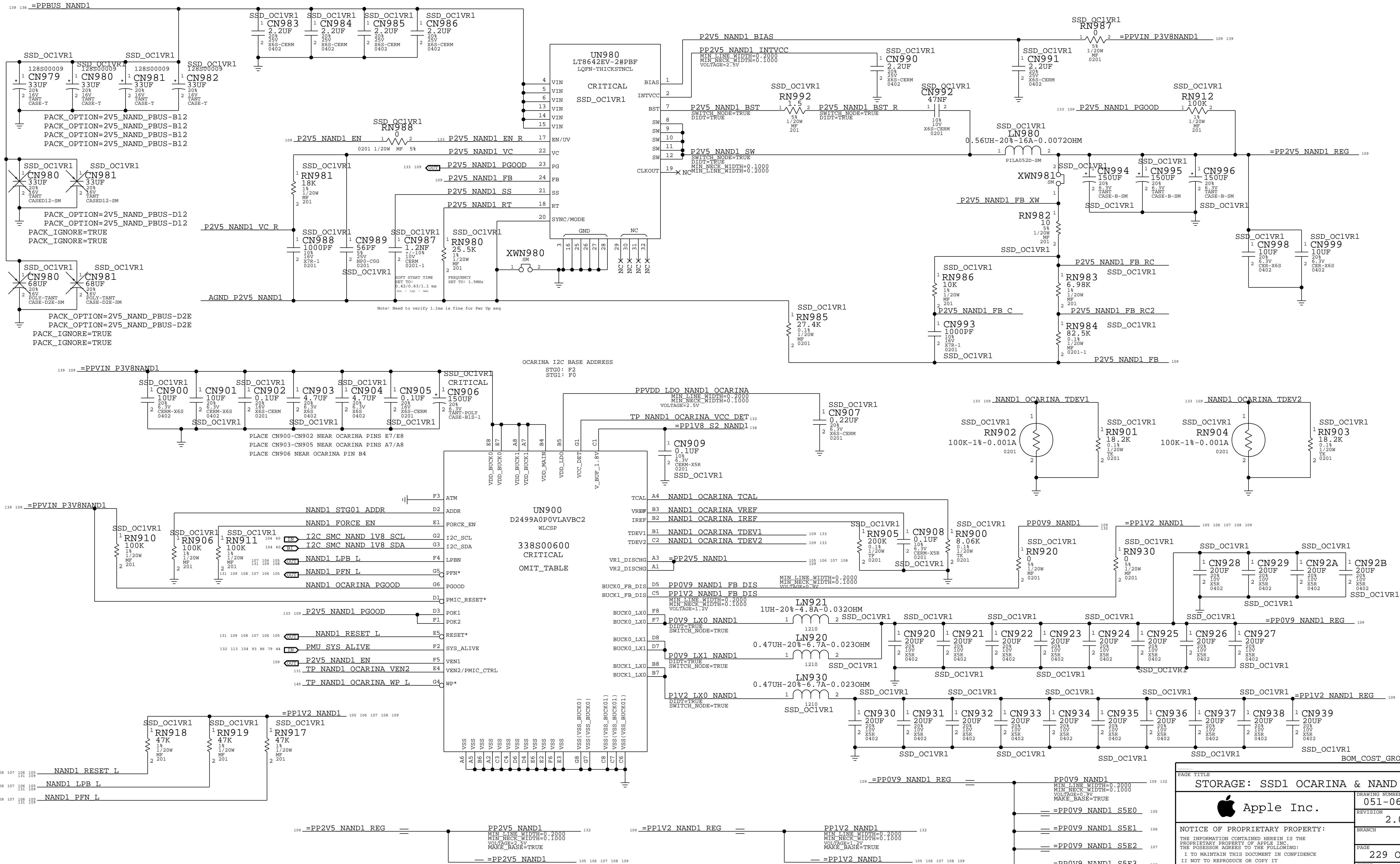
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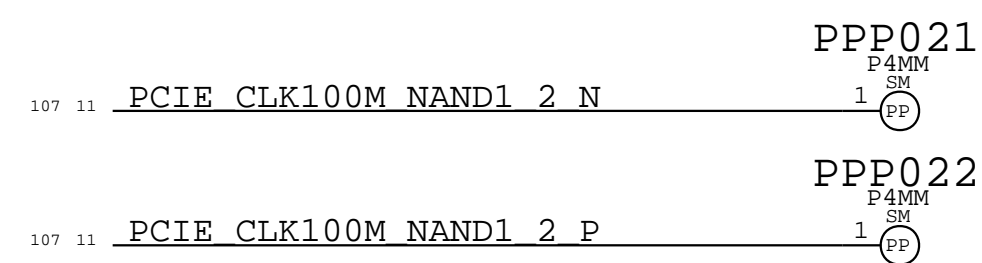
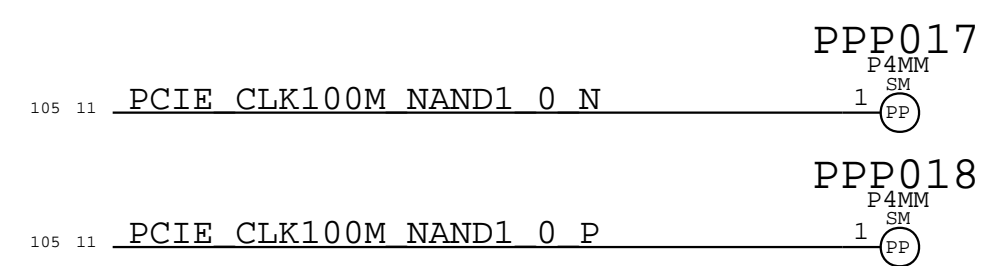
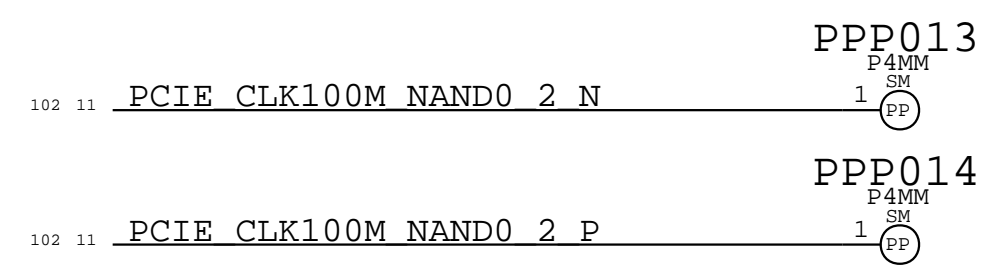
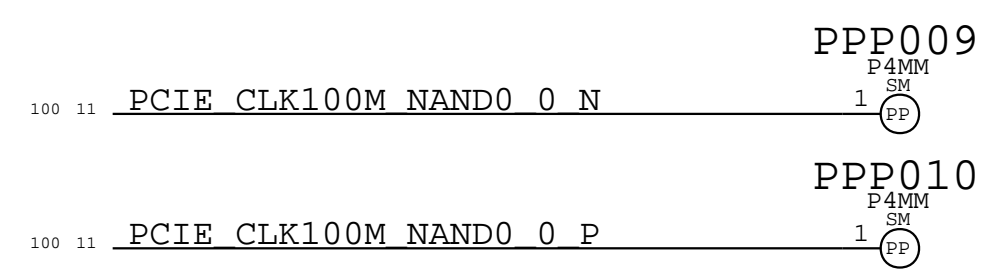
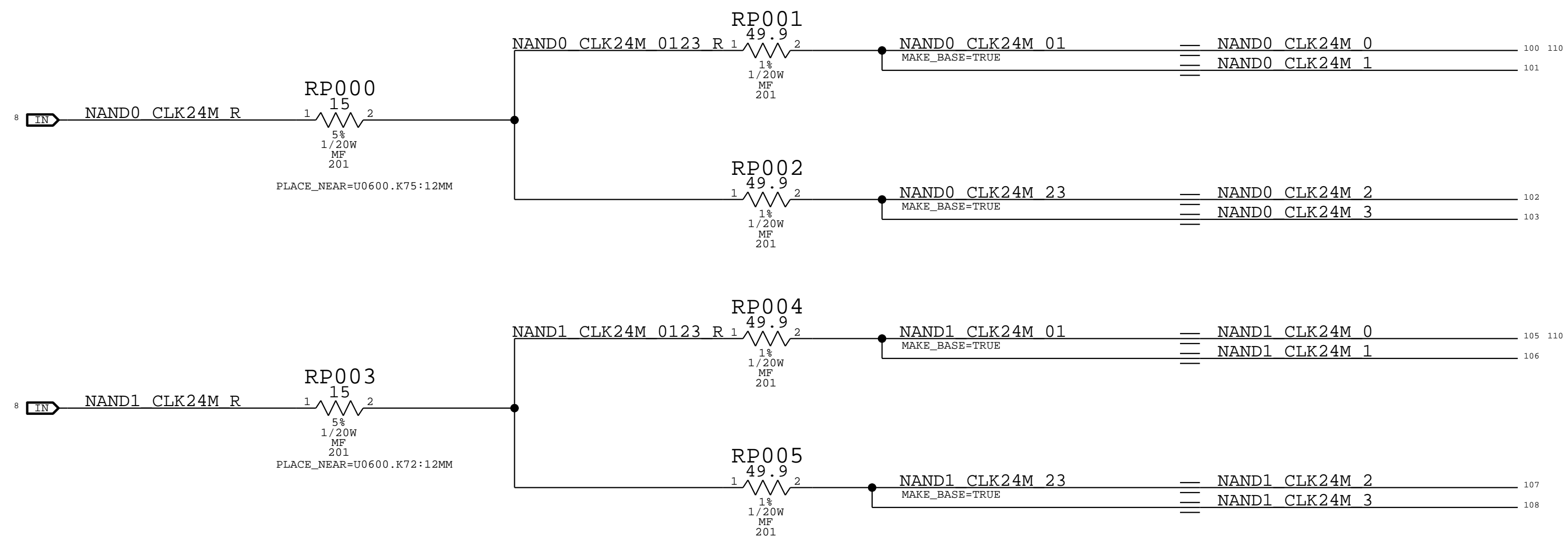
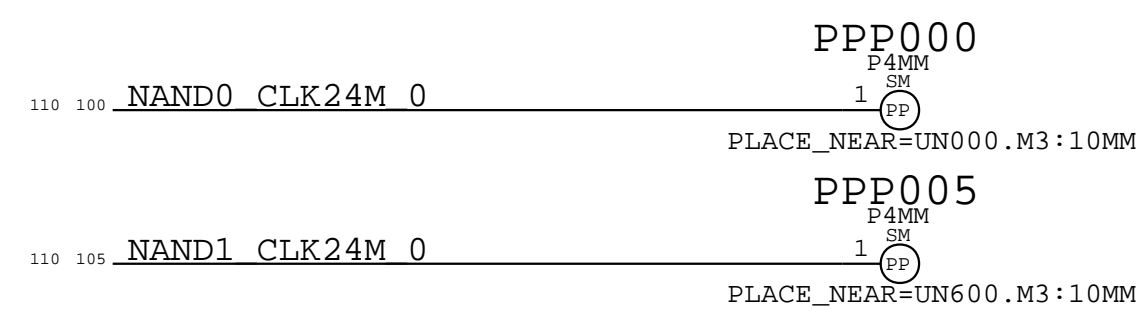
NAND1 S5E3



PAGE TITLE			
STORAGE: SSD1 S5E <3>			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-06558		D
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	2.0.0		
	BRANCH		
	PAGE		
	228 OF 998		
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	108 OF 156		

*** OK2INTEGRATE ***

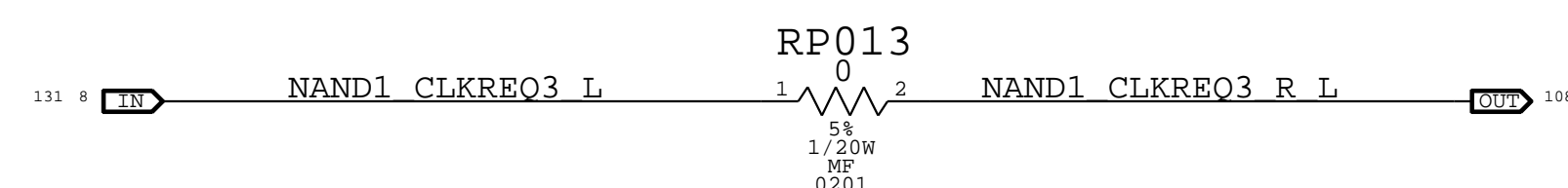
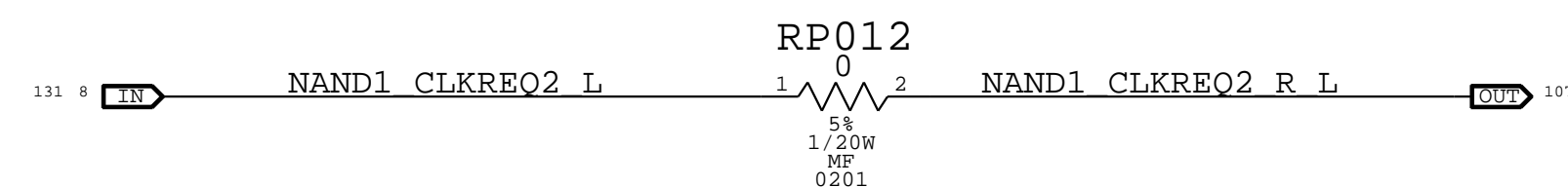
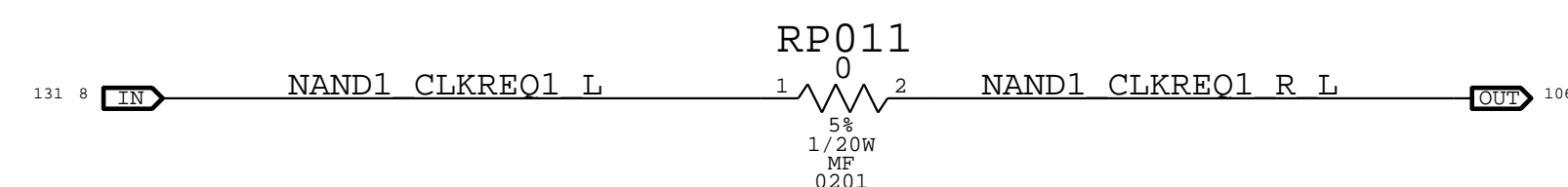
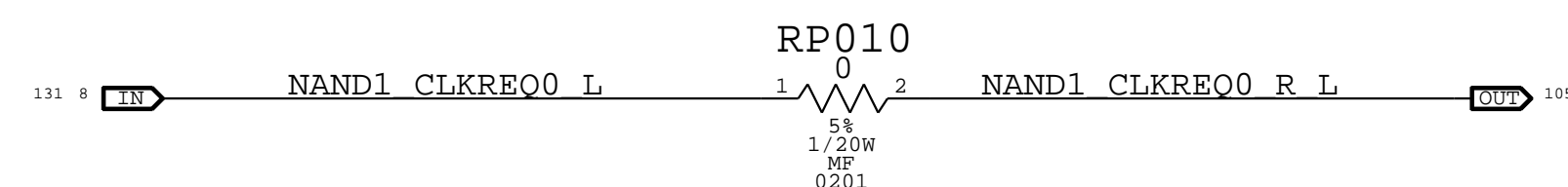
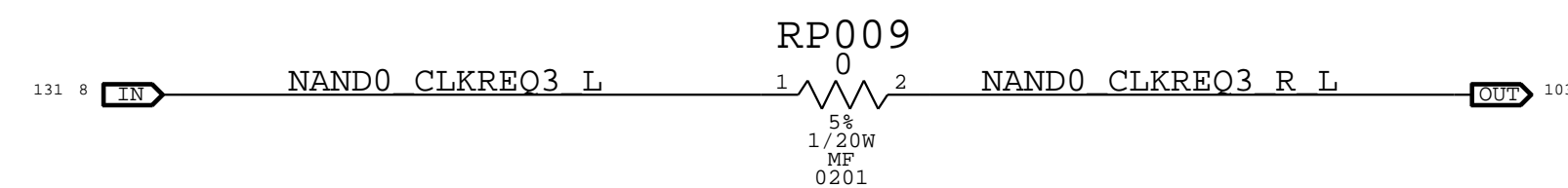
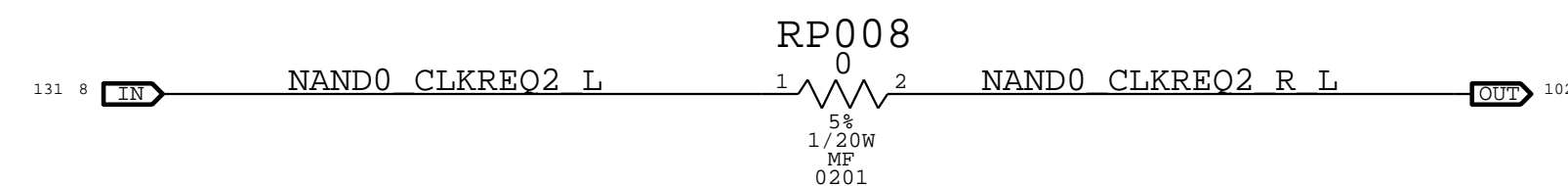
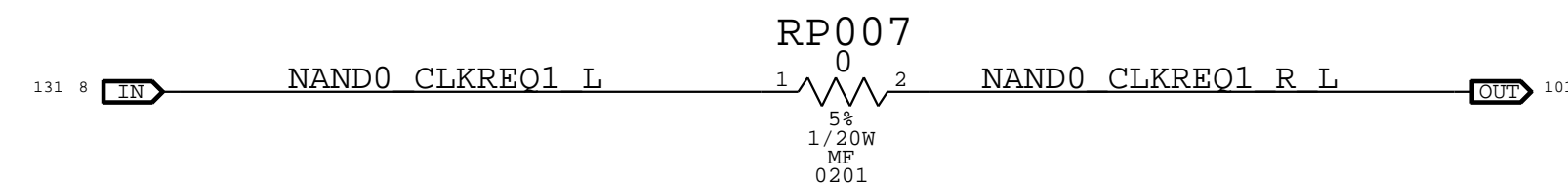
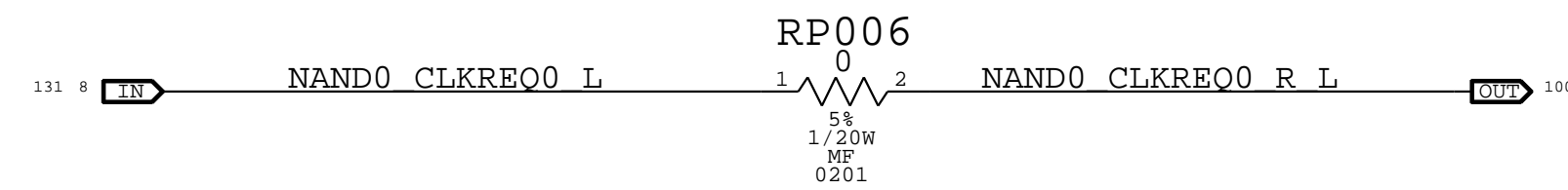





SSD 24M CLOCK TERMINATIONS

NAND CLKREQ SERIES RESISTORS

TODO: RES VALUES NOT FINAL



PAGE TITLE		
STORAGE: SSD SUPPORT		
 Apple Inc.	DRAWING NUMBER	SIZE
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	BRANCH	
	PAGE	
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	SHEET	
	110 OF 156	

BOM_COST_GROUP=SSD

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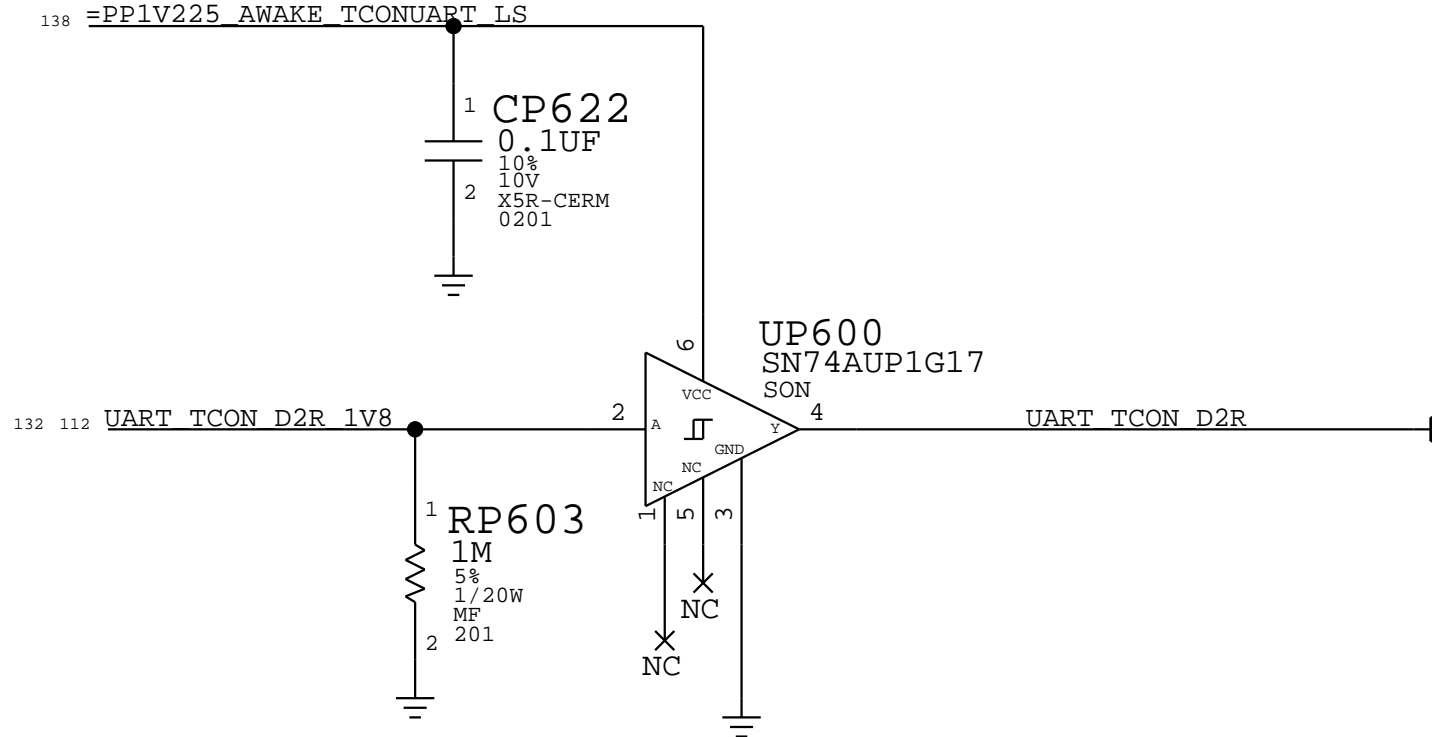
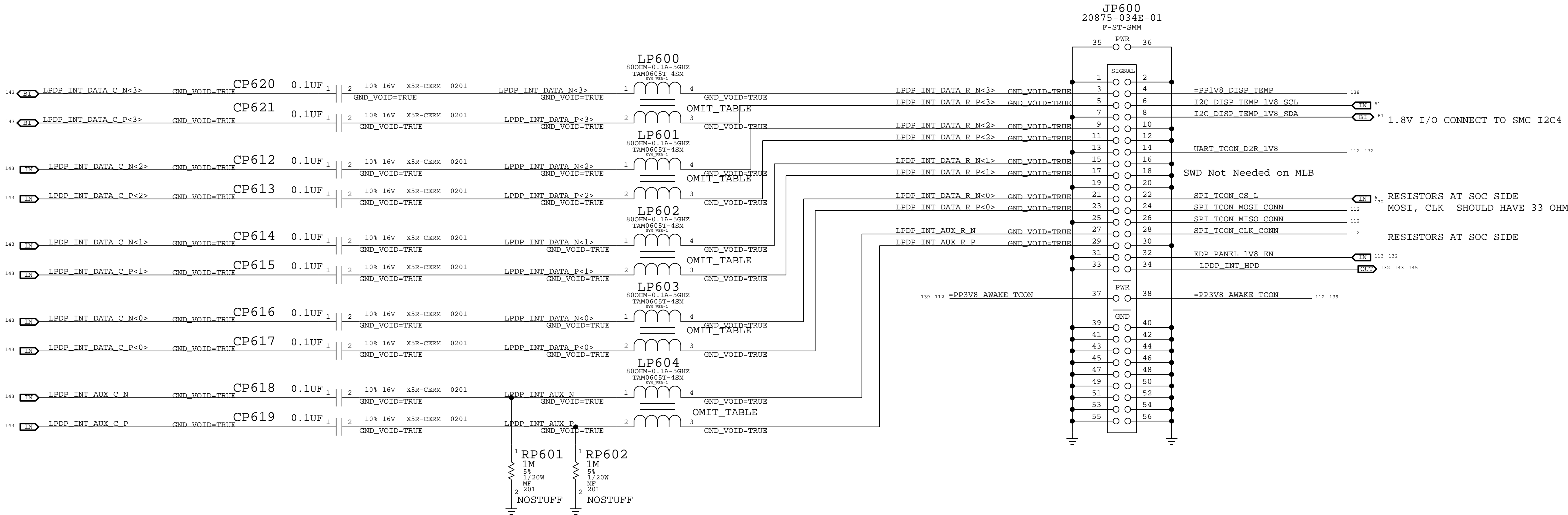
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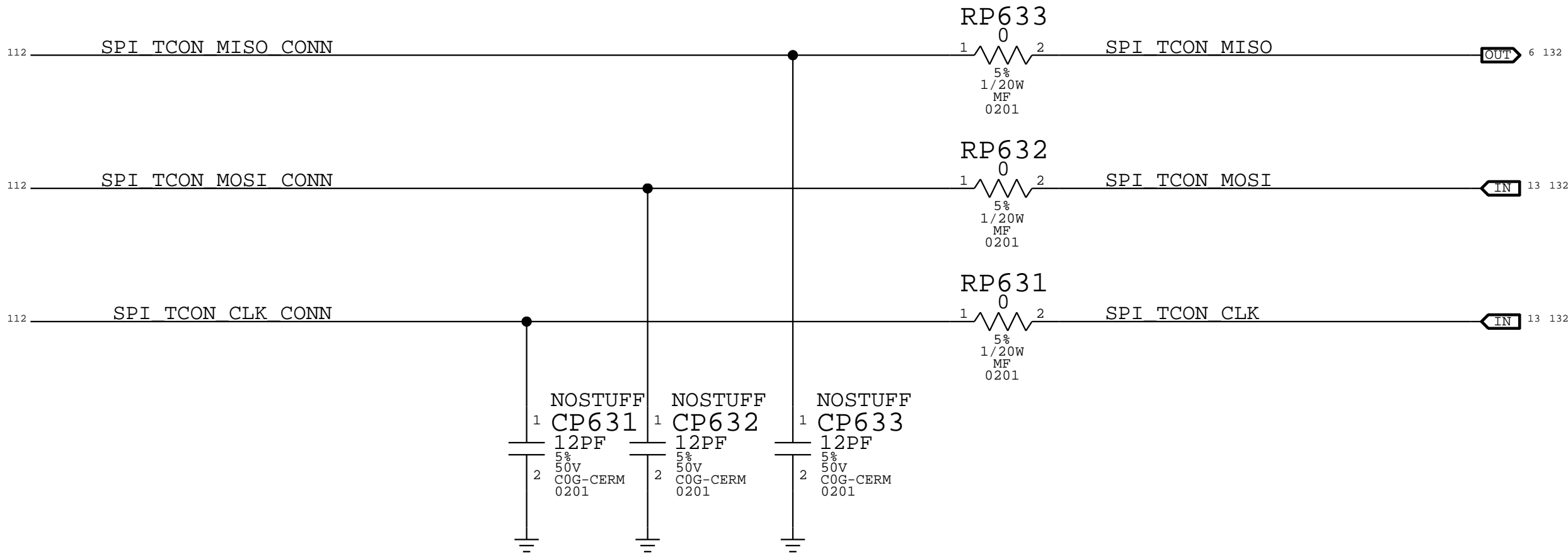
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A

APN: 516S00682



RC FILTER



CMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0943	5	FLTR,NOISE,8 OHMZ,2.6 OHM,100MA,0605	LP600-LP604	CRITICAL	

PAGE TITLE			DRAWING NUMBER			SIZE		
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						236 OF 998		
			SHEET			112 OF 156		

BOM_COST_GROUP=DISPLAY

*** OK2INTEGRATE ***

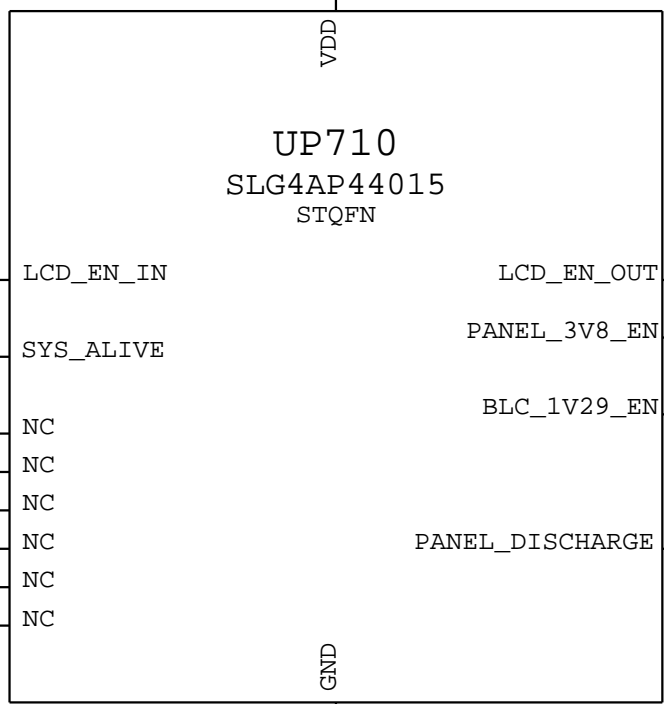
138 =PP3V8 AON LCD SW VIN

138 =PP1V8 AON LCD SW VIN

132 109 104 93 86 79 44

LCD_PWR_EN
PMU_SYS_ALIVE

NC
NC
NC
NC
NC
NC



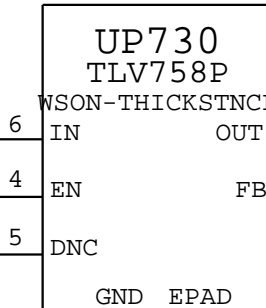
BYPASS=UP710::4MM
CP770
1.0UF
20%
10V
X5R-CERM
0201

LCD_EN_IN
SYS_ALIVE
LCD_EN_OUT
PANEL_3V8_EN
BLC_1V29_EN
PANEL_DISCHARGE

EDP_PANEL_1V8_EN
EDP_PANEL_PWR_EN
EDP_BKLT_1V29_EN
CONTROLS 1.29V LDO IN PMIC
EDP_PANEL_DISCHARGE

CP730
1.0UF
20%
6.3V
X5R
0201-1

CRITICAL



FB BLKT 2D

RP732
49.9K
1%
1/20W
MF
201

RP731
10K
1%
1/20W
MF
201

$V_{OUT} = V_{FB} * (1 + R1/R2)$
 $V_{OUT} = 0.55 * (1 + 49.9/10)$
 $V_{OUT} = 3.2945$

NOSTUFF
RP730
0
5%
1/16W
MF-LP
402

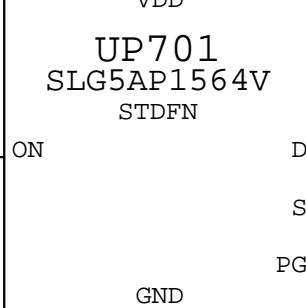
3V29 FEED TO BACKLIGHT

=PPBCON_SW_REG

CP731
0.1UF
10%
10V
X5R-CERM
0201

CP732
10UF
20%
10V
X5R-CERM
0402-7

CRITICAL



3V8 FEED TO MDB

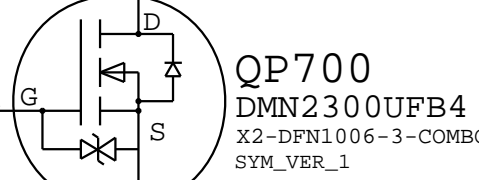
=PPMDB_SW_FET

CP718
0.1UF
10%
10V
X5R-CERM
0201

CP719
10UF
20%
10V
X5R-CERM
0402-7


RP700
300
5%
1/16W
MF-LP
402

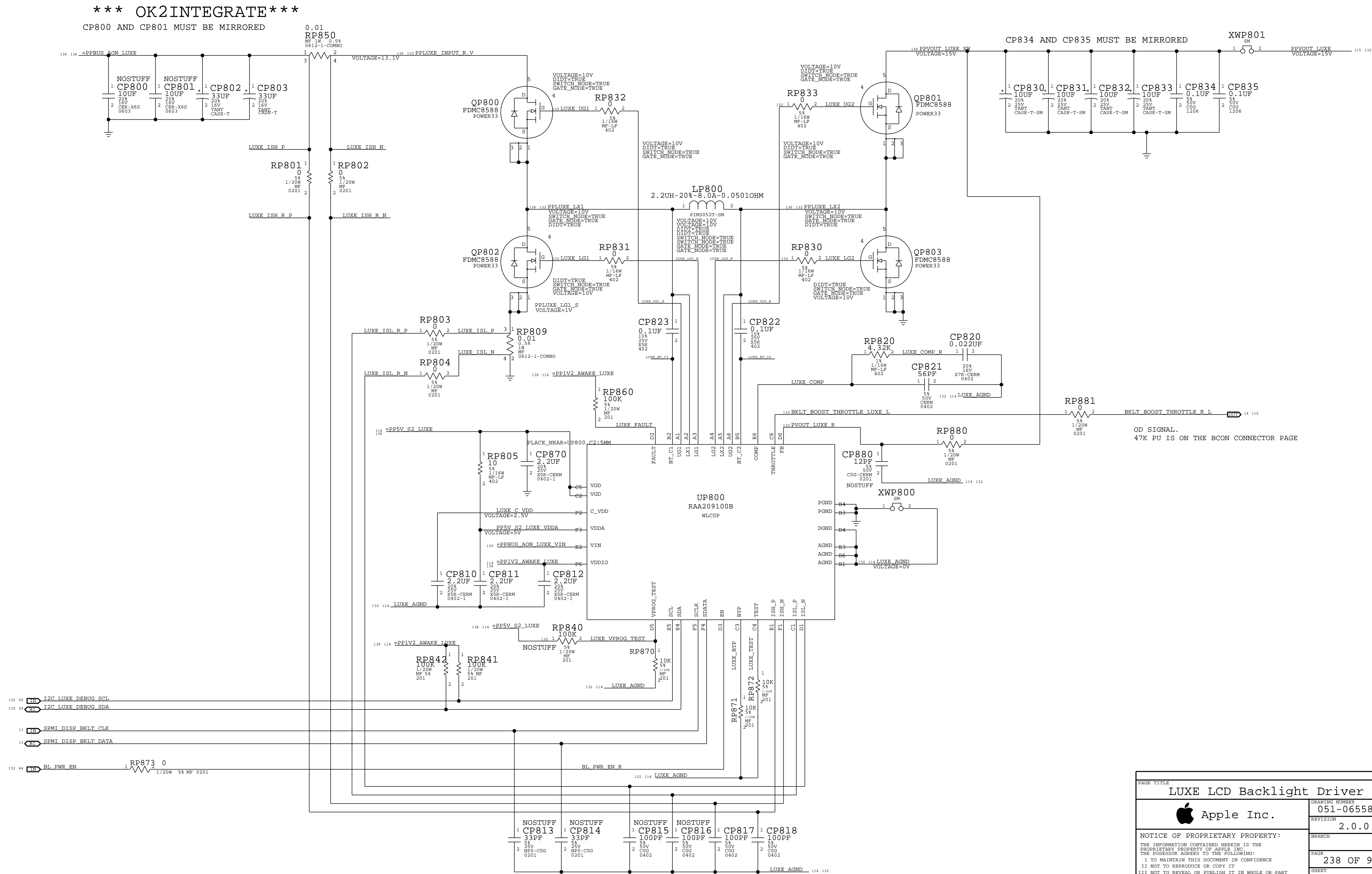
PPPANEL_PANEL_DISCHARGE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=4V




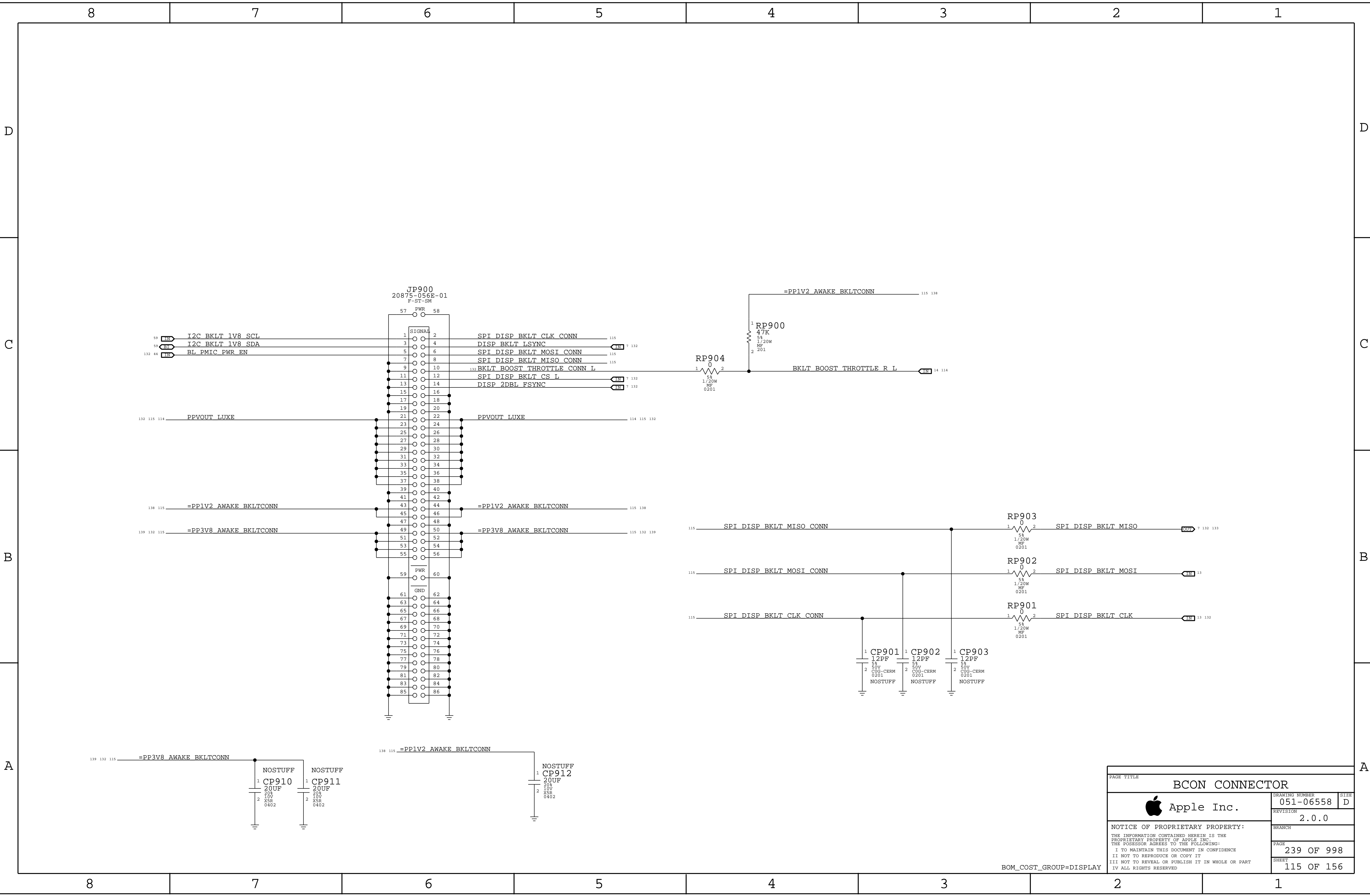
RP701
100K
5%
1/20W
MF
201


BOM_COST_GROUP=DISPLAY

PAGE TITLE		
DISPLAY POWER SEQUENCER		
 Apple Inc.	DRAWING NUMBER	051-06558
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	PAGE	237 OF 998
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PAGE TITLE			
LUXE LCD Backlight Driver			
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	BRANCH		
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PAGE TITLE		
BCON CONNECTOR		
 Apple Inc.	DRAWING NUMBER	051-06558
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	SHEET 115 OF 156	

BOM_COST_GROUP=DISPLAY

D

D



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BOM_COST_GROUP=SOC

8

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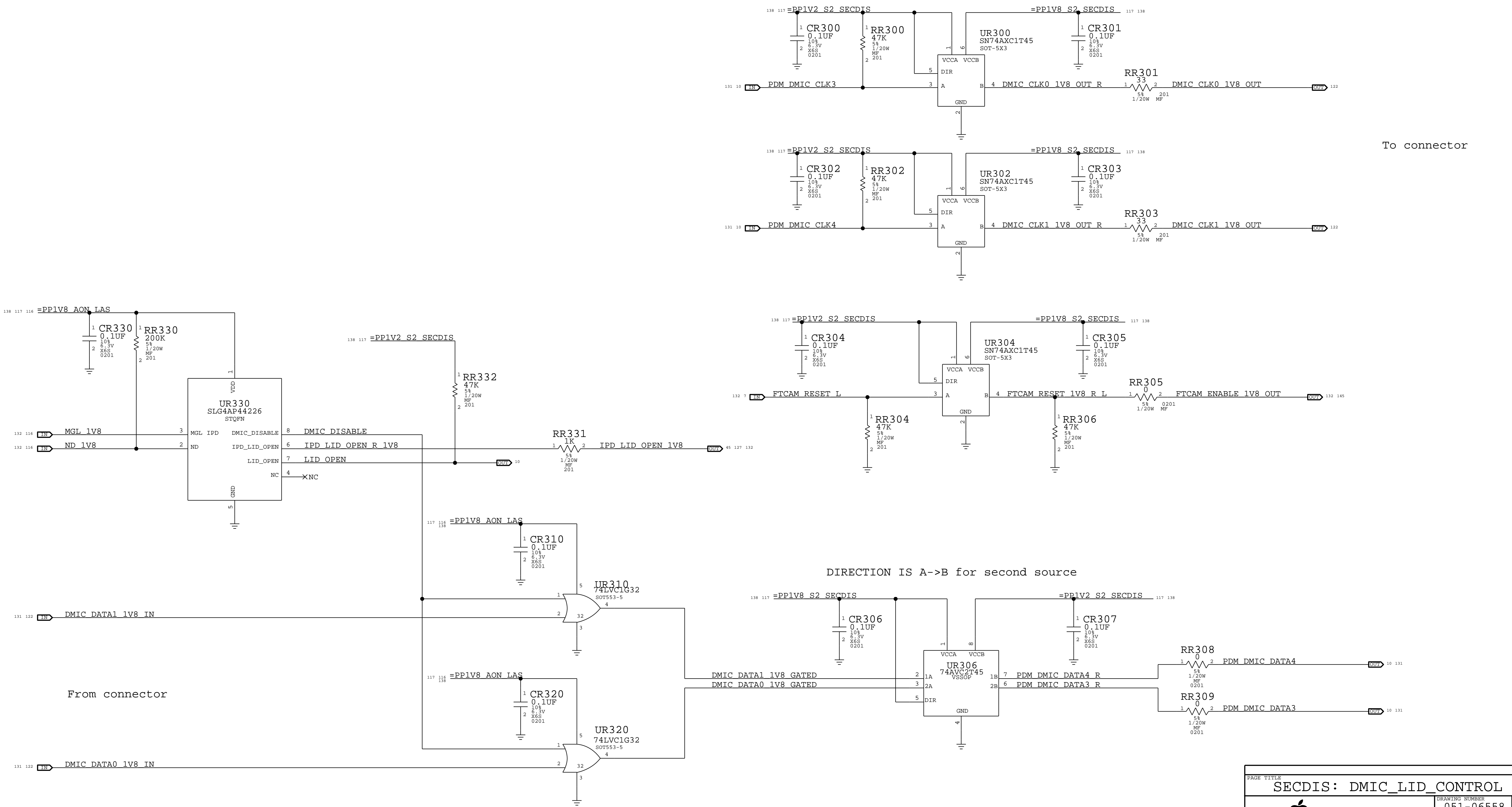
3


2

1

*** OK2INTEGRATE ***

Level Shifter - DMIC & FTCAM

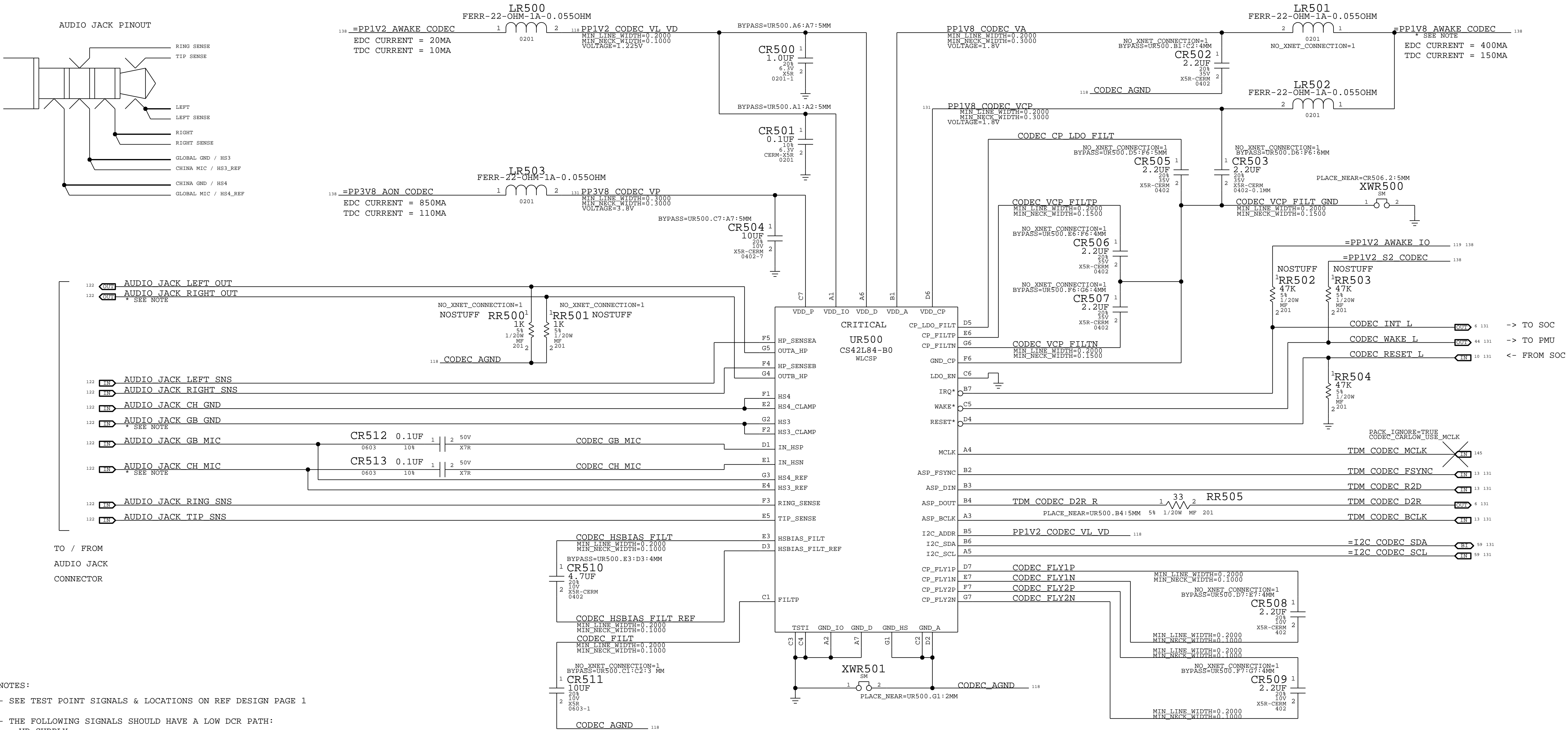


PAGE TITLE		
SECDIS: DMIC_LID_CONTROL		
 Apple Inc.	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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BOM_COST_GROUP=SOC

*** OK2INTEGRATE ***


CARLOW CODEC I2C ADDRESS	
ADDR PIN	ADDRESS
0R TO GND	0X48
100K TO GND	0X49
100K TO VDDIO	0X4A
0R TO VDDIO	0X4B <--



NOTES:

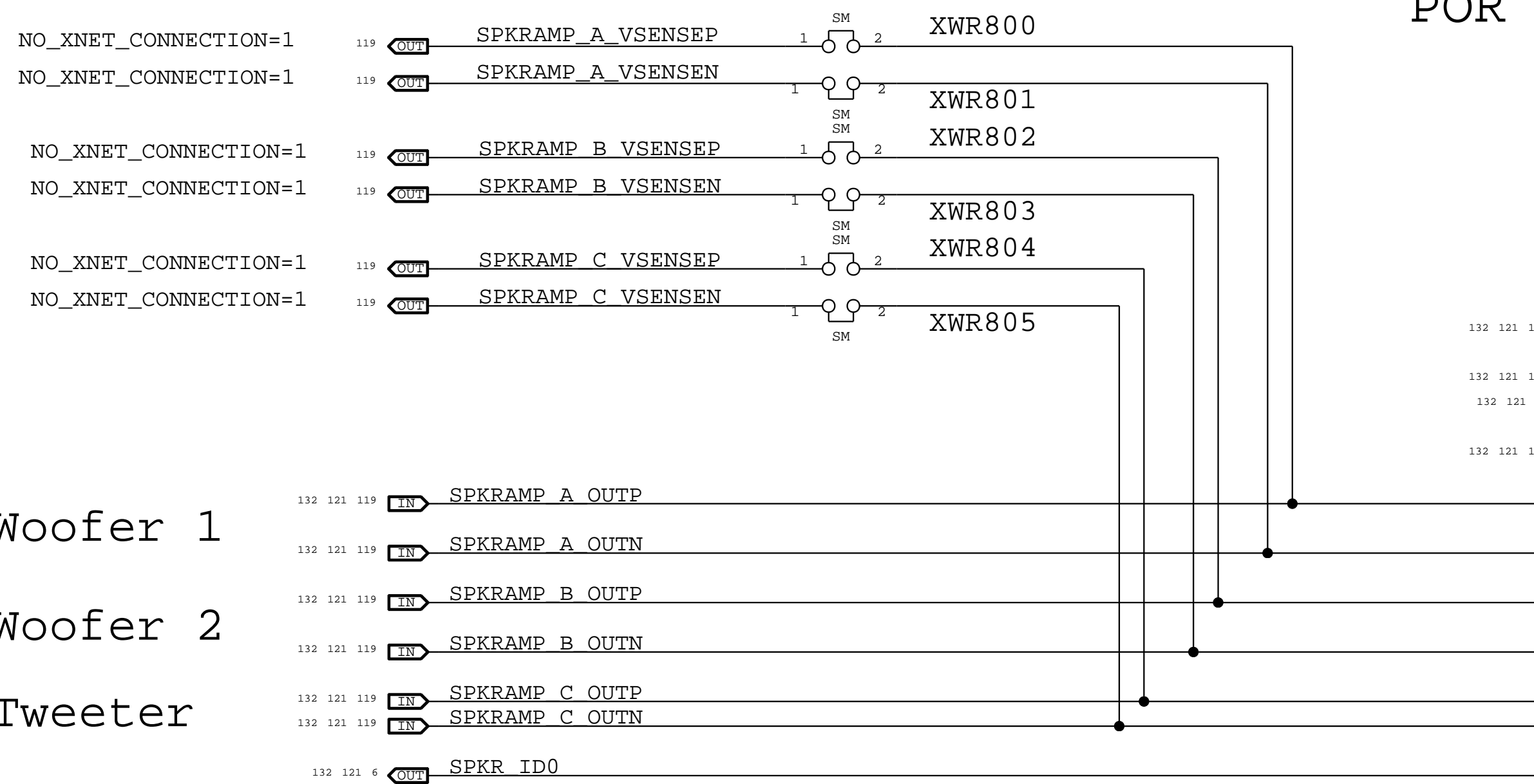
- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1
- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
 - VP SUPPLY
 - VCP SUPPLY
 - AUDIO_JACK_LEFT/RIGHT_OUT
 - AUDIO_JACK_GB/CH_GND
- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.
- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP WHEN THE OTHER RAILS GO DOWN)
VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
3.1UA (1V8 OFF, RST# LOW)
TBD (1V8 ON, RST# LOW)
37UA (1V8 OFF, RST# HIGH)

CARLOW B0 SILICON

SYNC_MASTER=TS58_REF_CODEC_CARLOW_1.0.0		SYNC_DATE=06/05/2020	
PAGE TITLE			
AUDIO JACK CODEC			
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	REVISION	2.0.0	
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		PAGE	245 OF 998
		SHEET	118 OF 156

BOM_COST_GROUP=AUDIO

LEFT AUDIO SPEAKER CONNECTOR

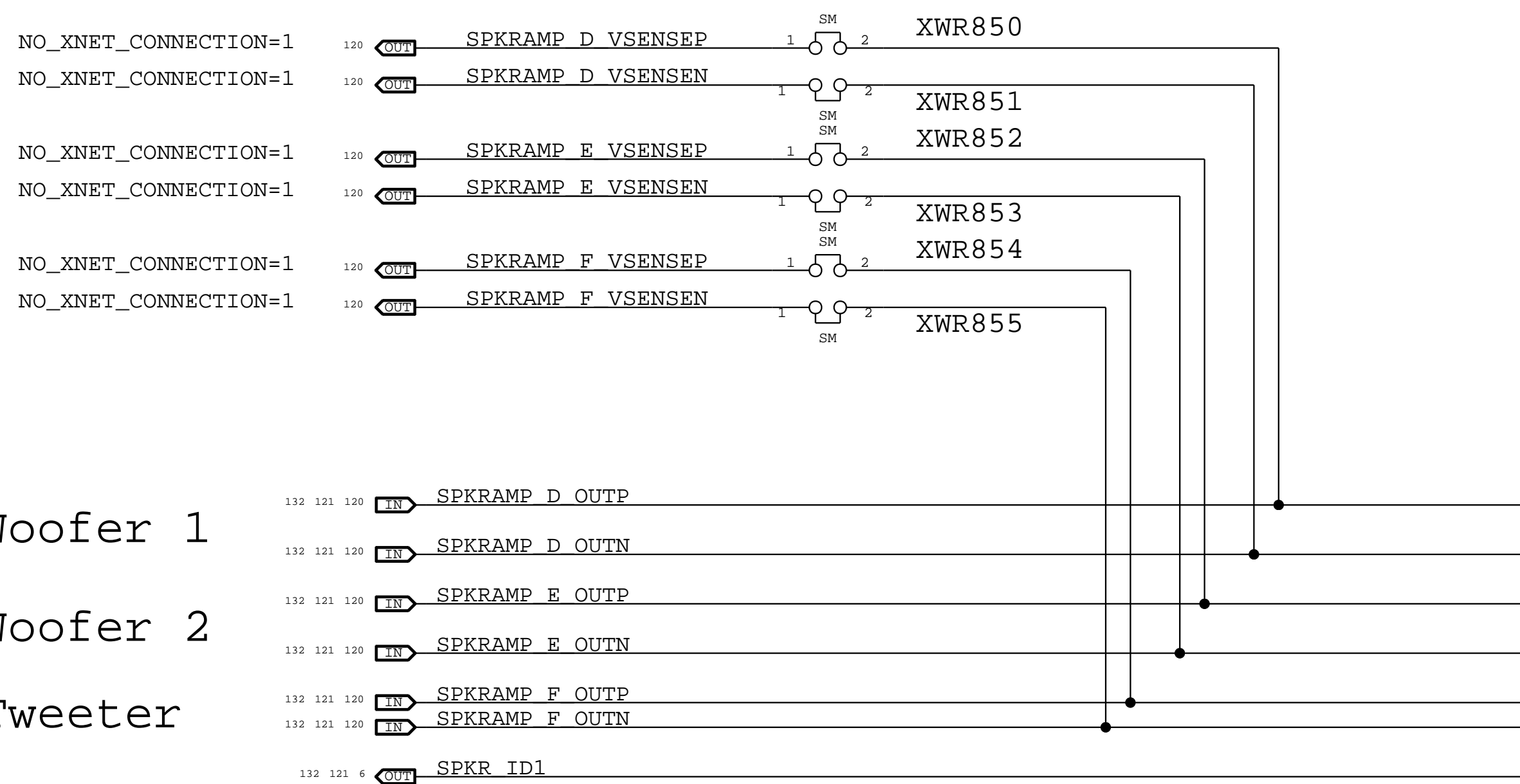


L Woofer 1

L Woofer 2

L Tweeter

RIGHT AUDIO SPEAKER CONNECTOR

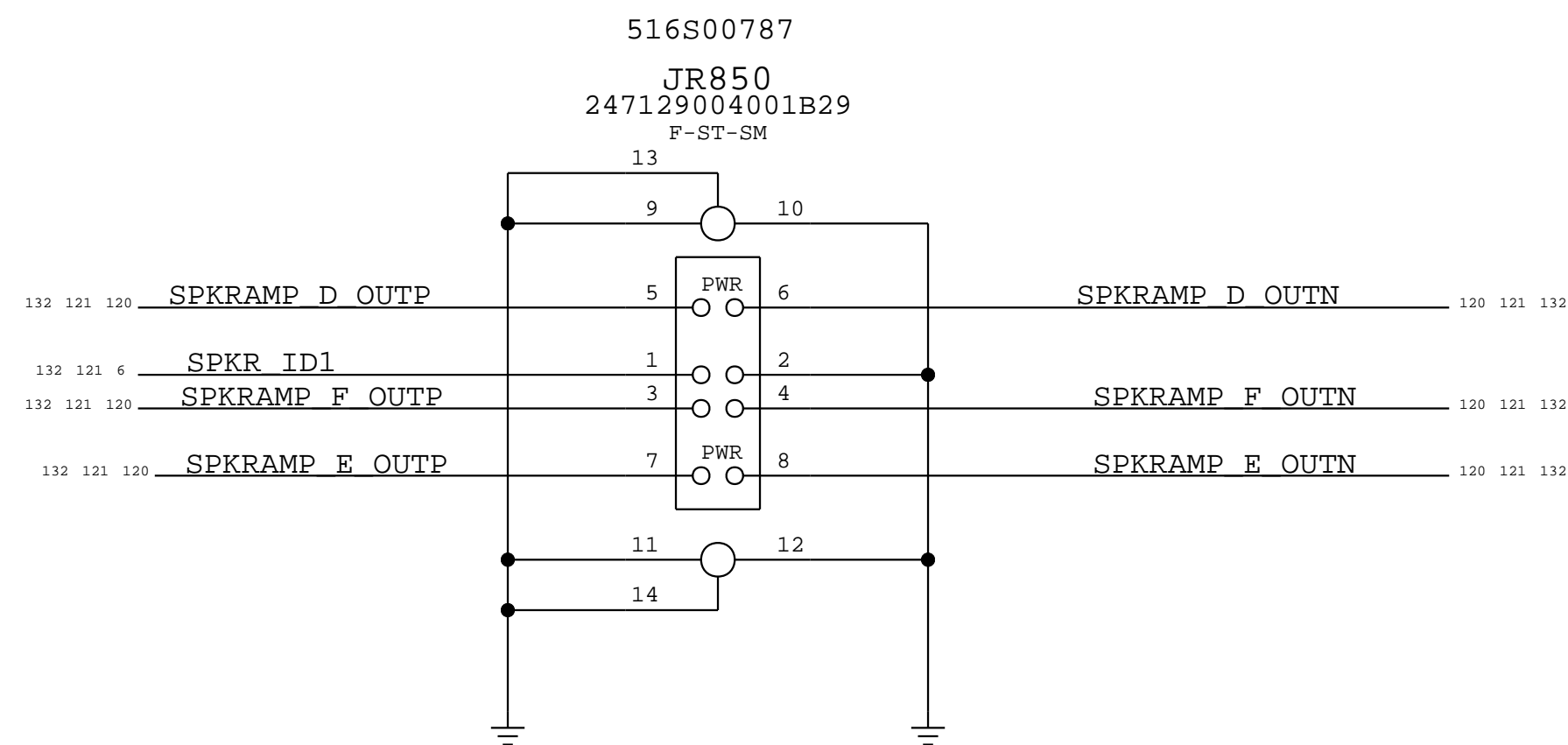
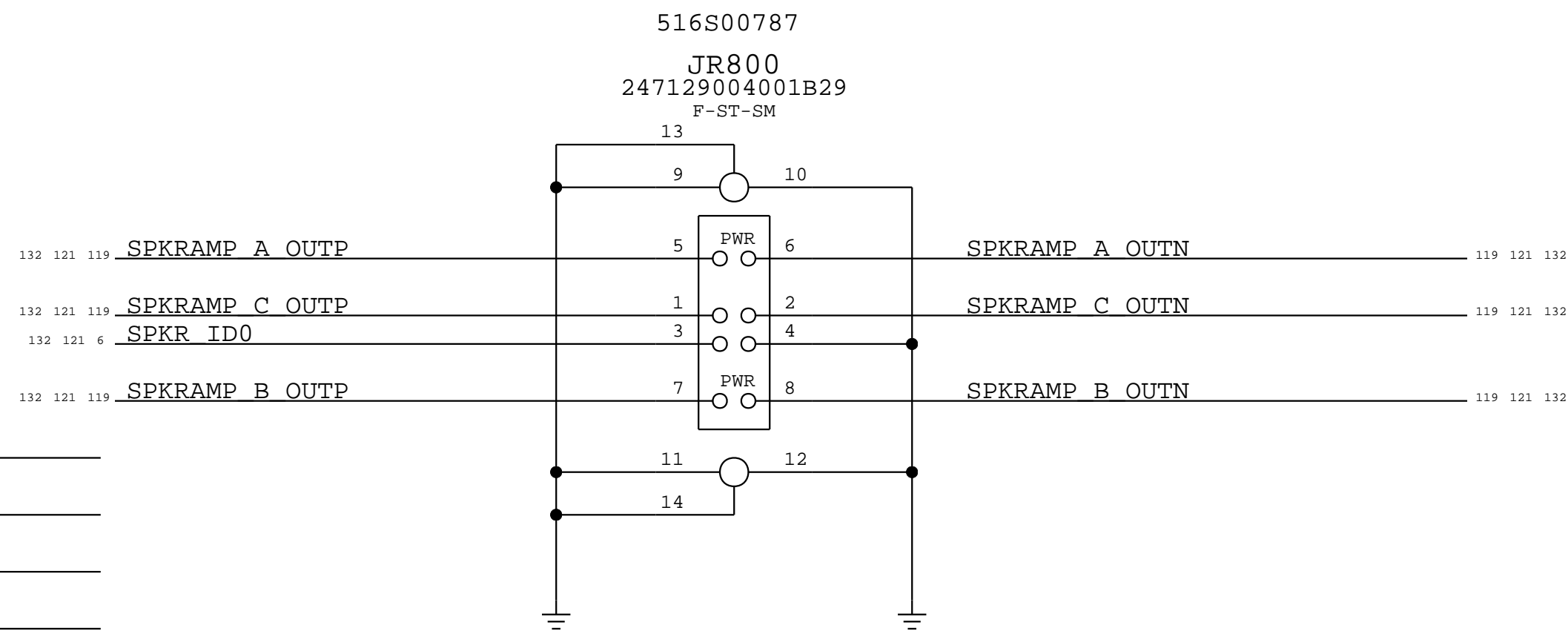


R Woofer 1

R Woofer 2

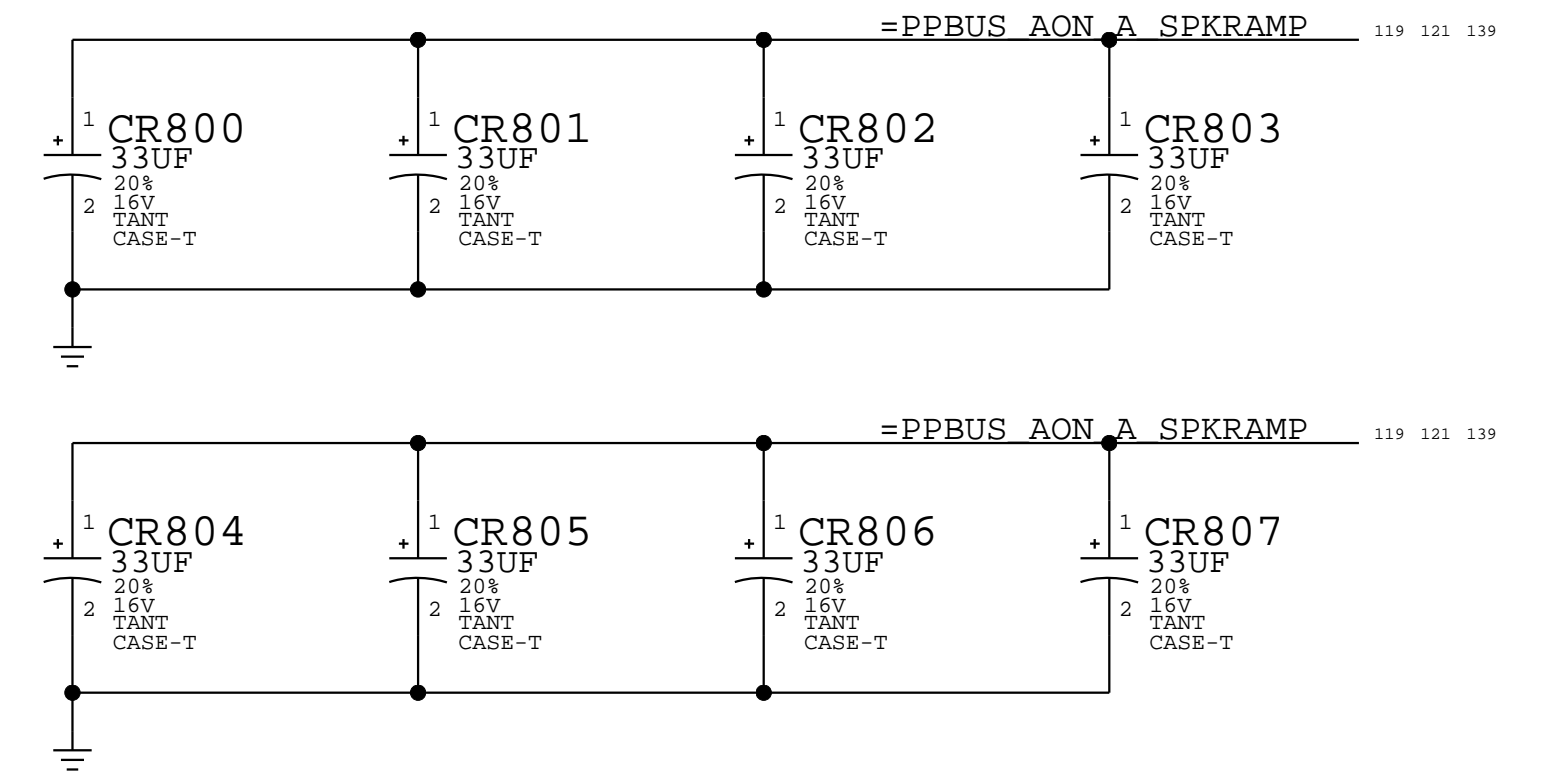
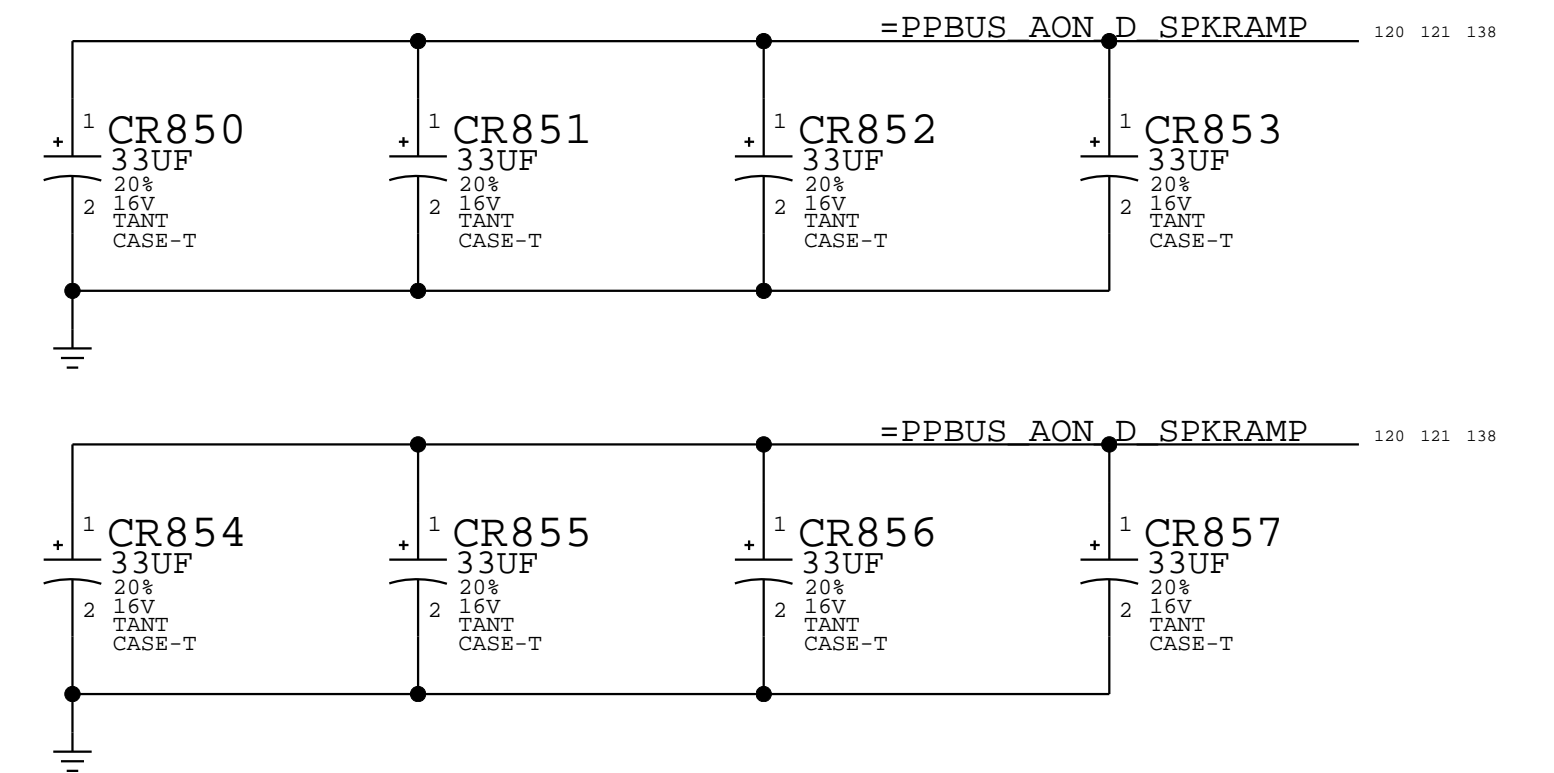
R Tweeter

J152 CONN APN:518S00818 FOR P0.
J316 CONN APN:516S00690 FOR P1.
POR COST CONN APN:516S00787 FOR P1C.P2S

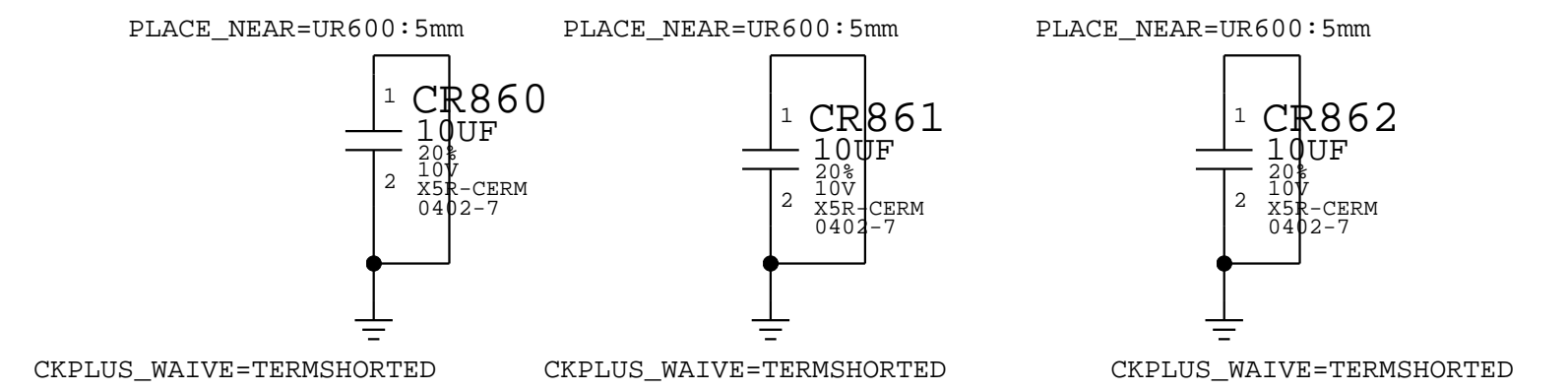



LEFT AMPLIFIERS

BULK CAPACITANCE

RIGHT AMPLIFIERS
BULK CAPACITANCE

DUMMY 0201 CAPS



FORM 24-00000-000000			
PAGE TITLE			
AUDIO CONNECTORS: AMPS			
 Apple Inc.	DRAWING NUMBER		SIZE
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	BRANCH		
	PAGE		
	248 OF 998		
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	121 OF 156		

BOM_COST_GROUP=AUDIO

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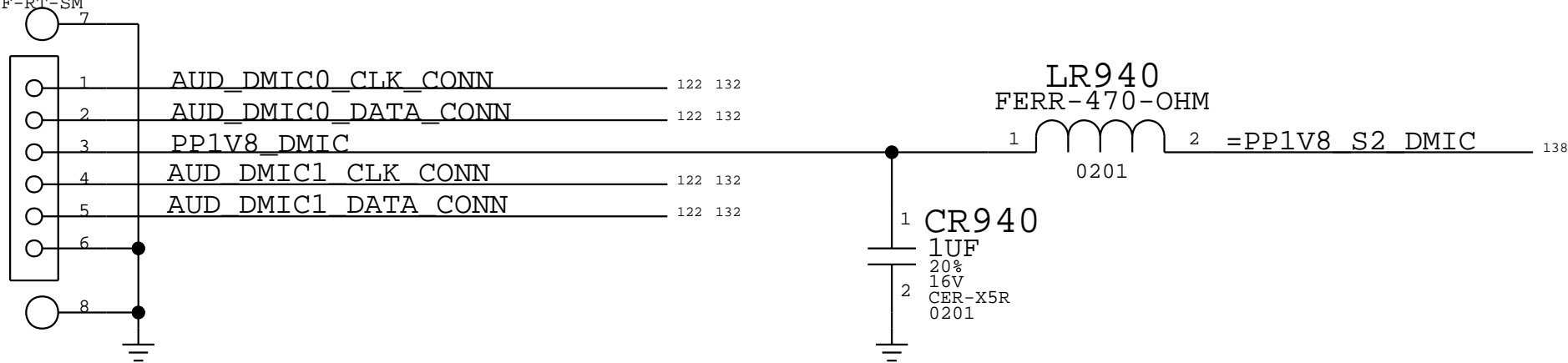
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Digital Mic Flex Connector

APN: 518S0818
JR940
FF14A-6C-R11DL-B-3H



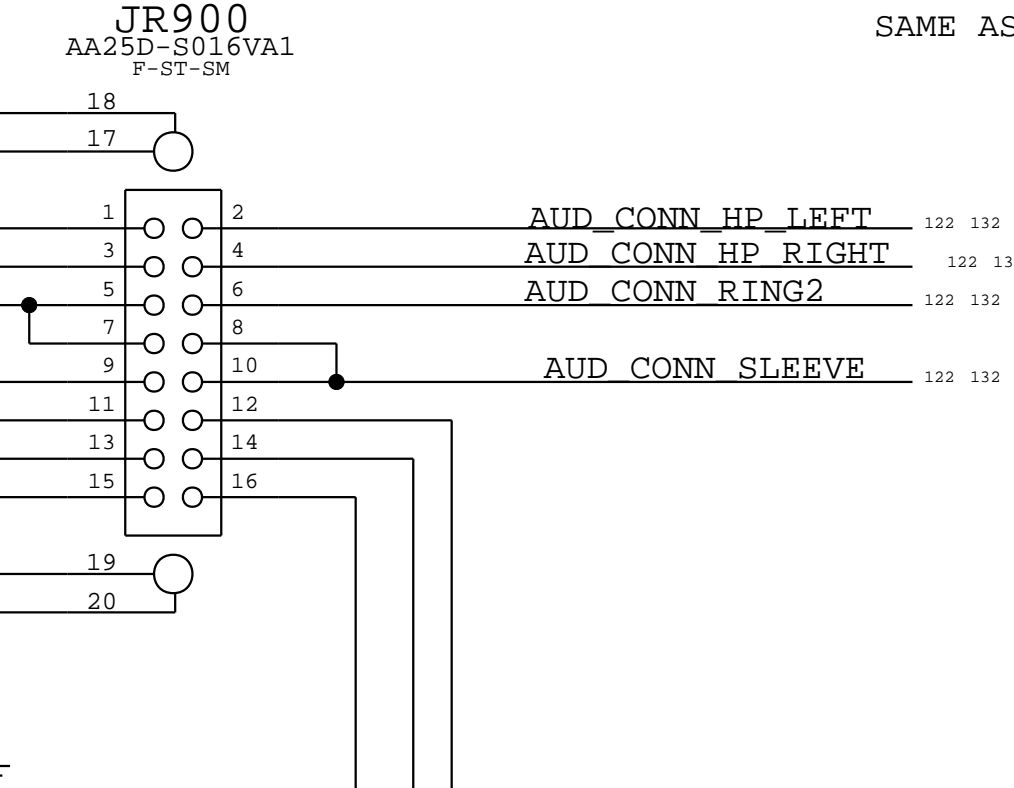
TODO: Check if zero ohms between connector an SECDIS are required

132	122	AUD_DMIC0_CLK_CONN	MAKP_BASE=TRUE	==	DMIC CLK0 1V8 OUT	117
132	122	AUD_DMIC0_DATA_CONN	MAKP_BASE=TRUE	==	DMIC DATA0 1V8 IN	117 131
132	122	AUD_DMIC1_CLK_CONN	MAKP_BASE=TRUE	==	DMIC CLK1 1V8 OUT	117
132	122	AUD_DMIC1_DATA_CONN	MAKP_BASE=TRUE	==	DMIC DATA1 1V8 IN	117 131

Audio Jack Flex Connector

PART_NUMBER=516S1181

APN: 516S1181 ,MATINGM PLUG APN:516S1180
SAME AS J214

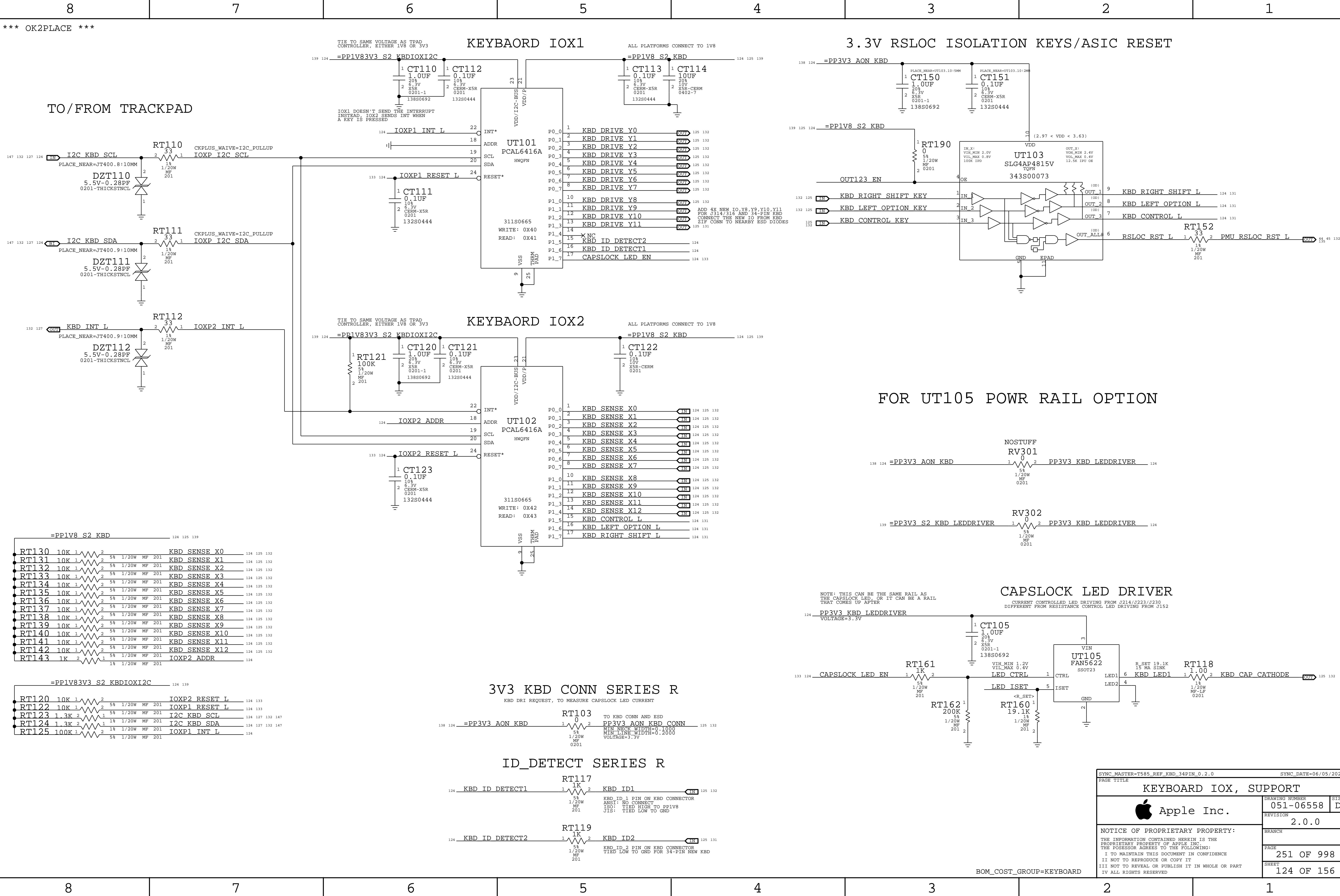


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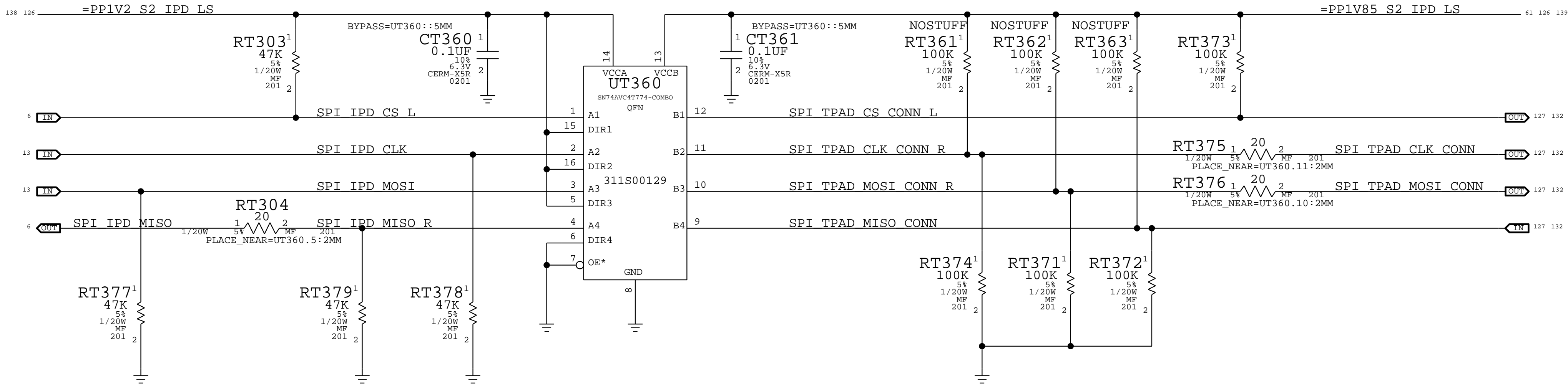
LAST CHANGE: Wed Feb 18 17:12:24 2015		
PAGE TITLE		
Audio Flex Connectors		
	DRAWING NUMBER	051-06558
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	PAGE	249 OF 998
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BEN IC: KEYBOARD LED DRIVER





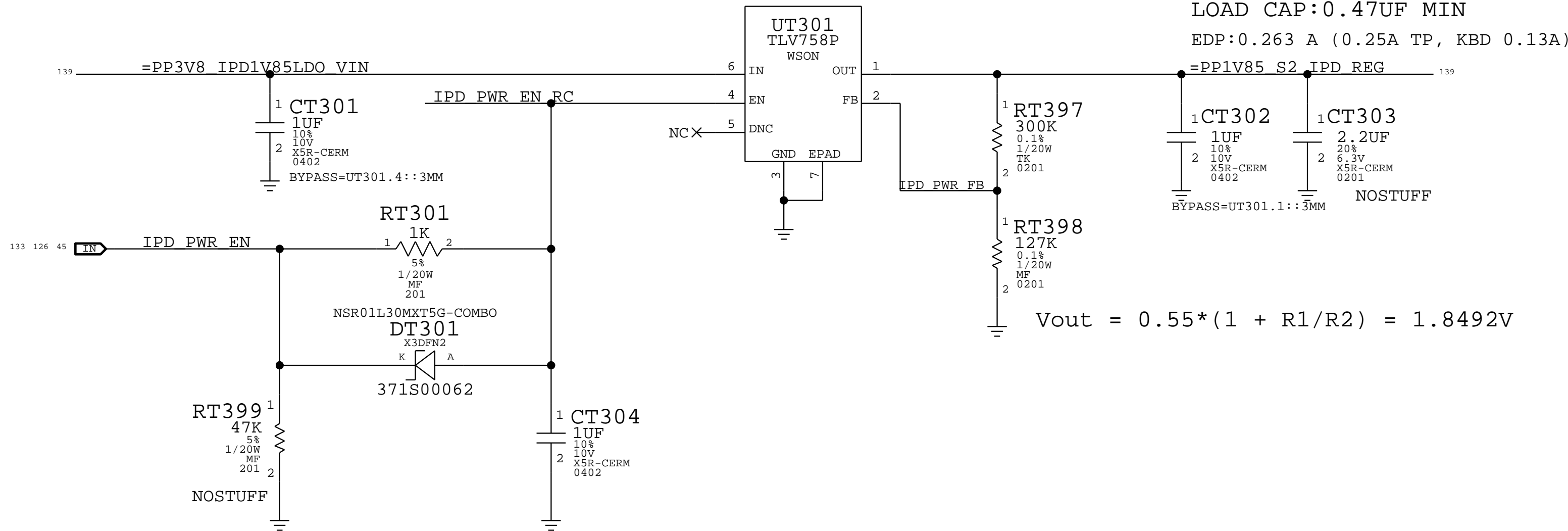
TRACKPAD SPI BUS LEVEL SHIFTER (+1.2V TO +1.8V)



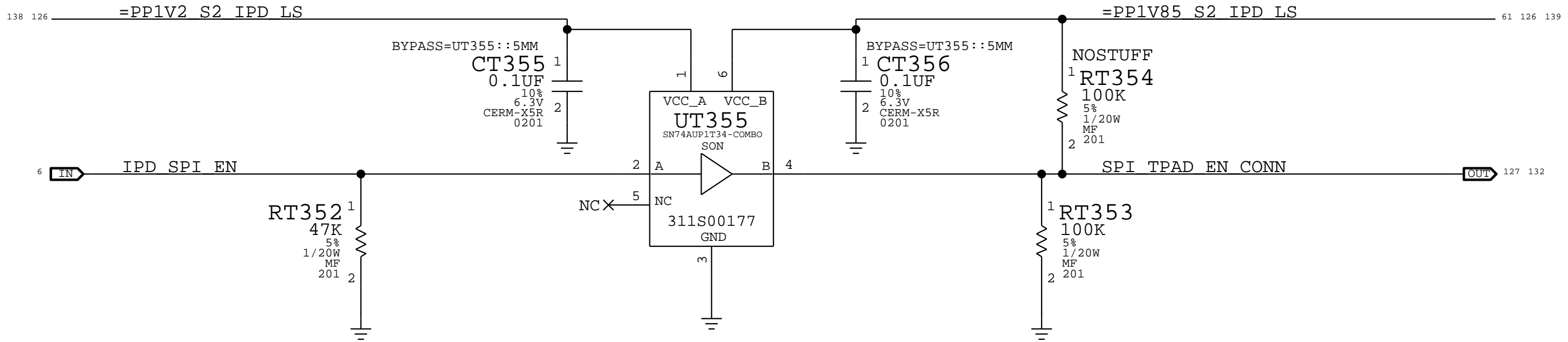
SN74AVC4T774 Truth Table

CTRL INPUTS		OUTPUT CIRCUITS		OPERATION
/OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

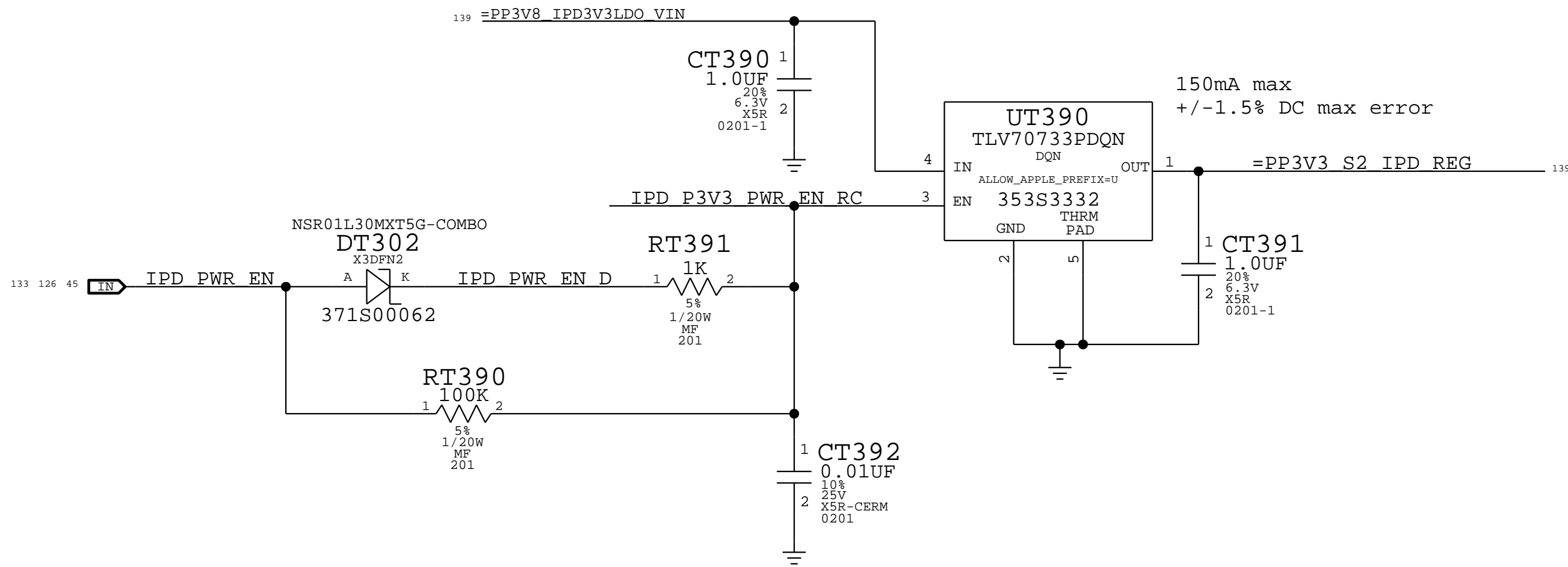
IPD LDO
1.85 V FOR TRACKPAD AND KEYBOARD IOX



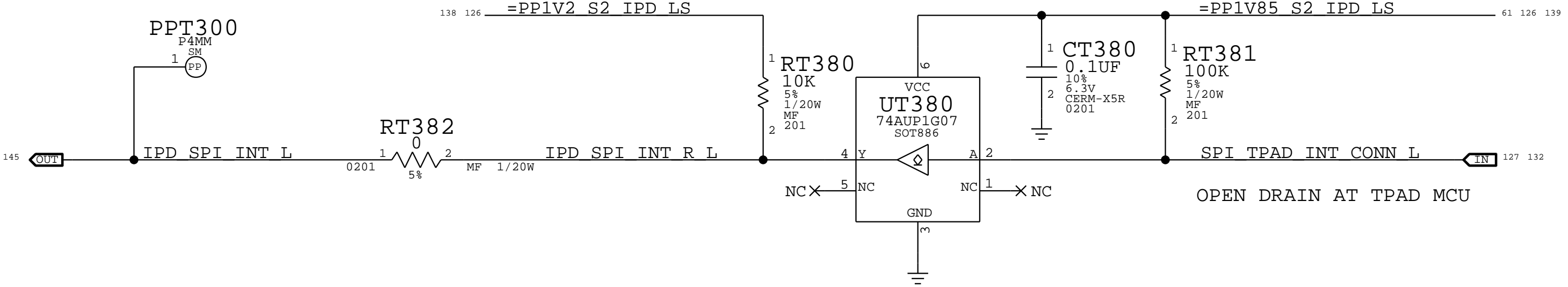
TRACKPAD SPI ENABLE LEVEL SHIFTER




3.3V S2 LDO FOR TPAD



IPD SPI INTERRUPT LEVEL SHIFTER



TRACKPAD SUPPORT

 Apple Inc.

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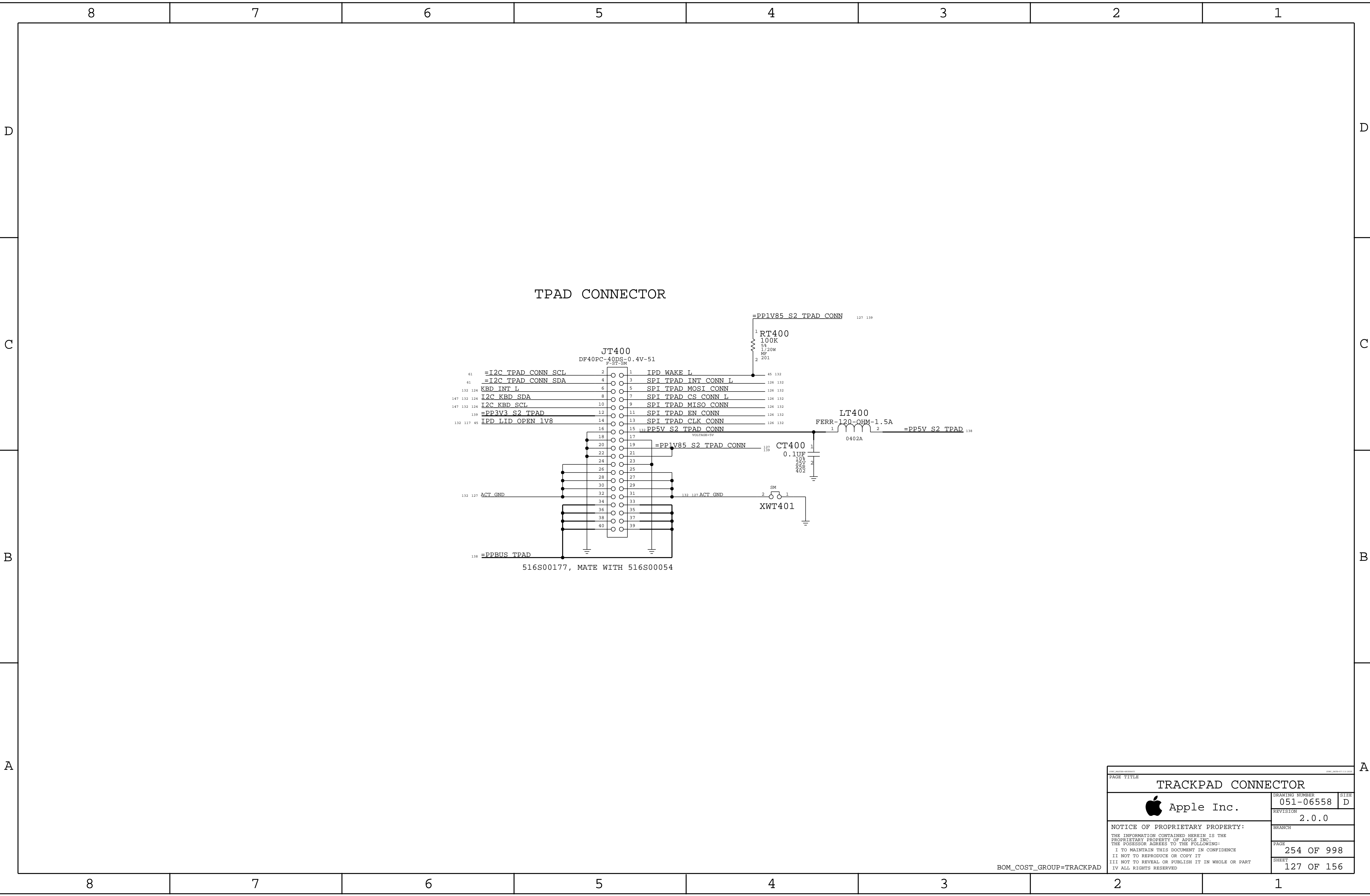
BRANCH

PAGE
253 OF 998

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126 OF 156

SIZE
D

BOM_COST_GROUP=TRACKPAD

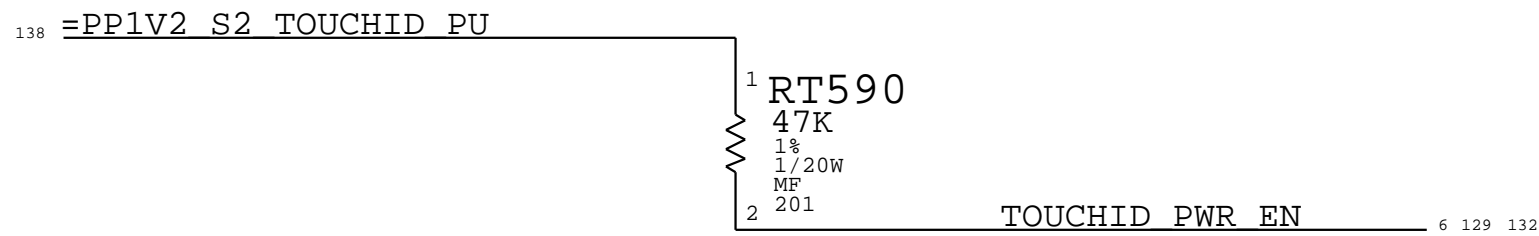
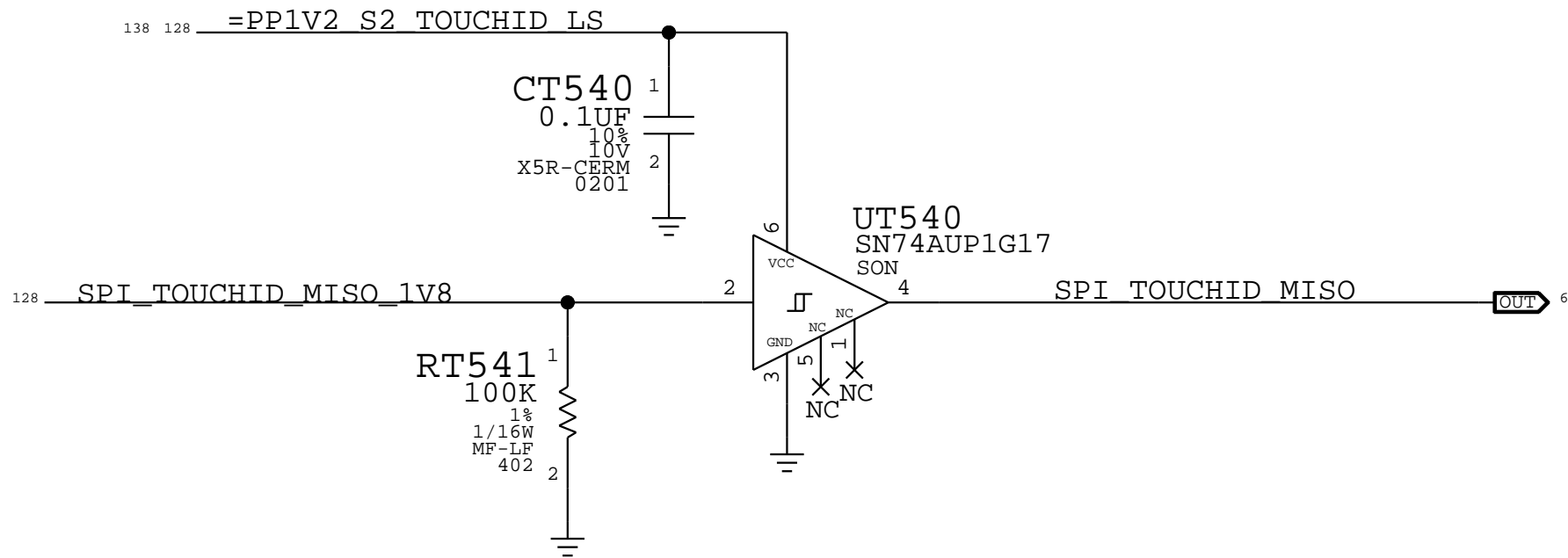
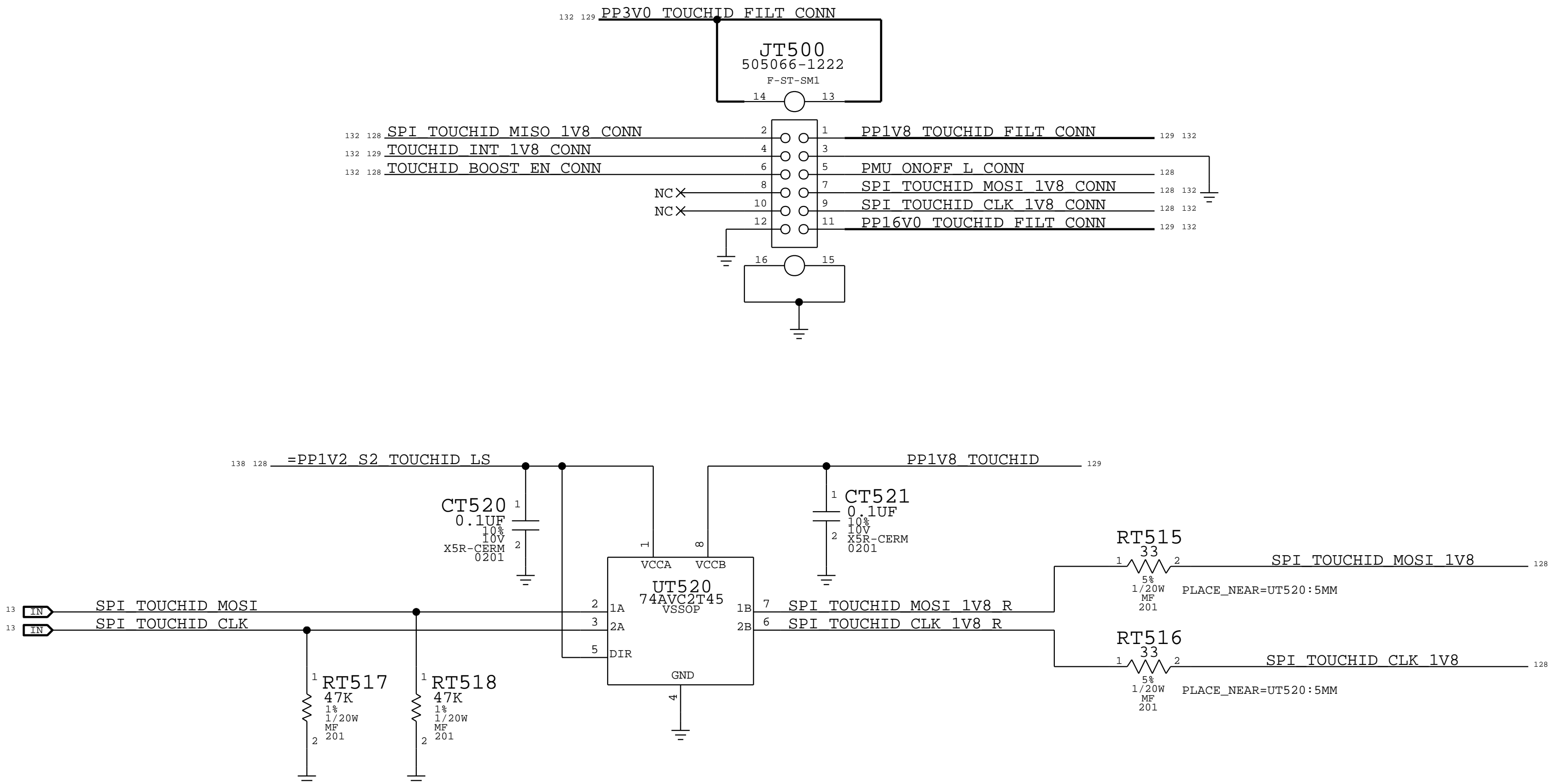
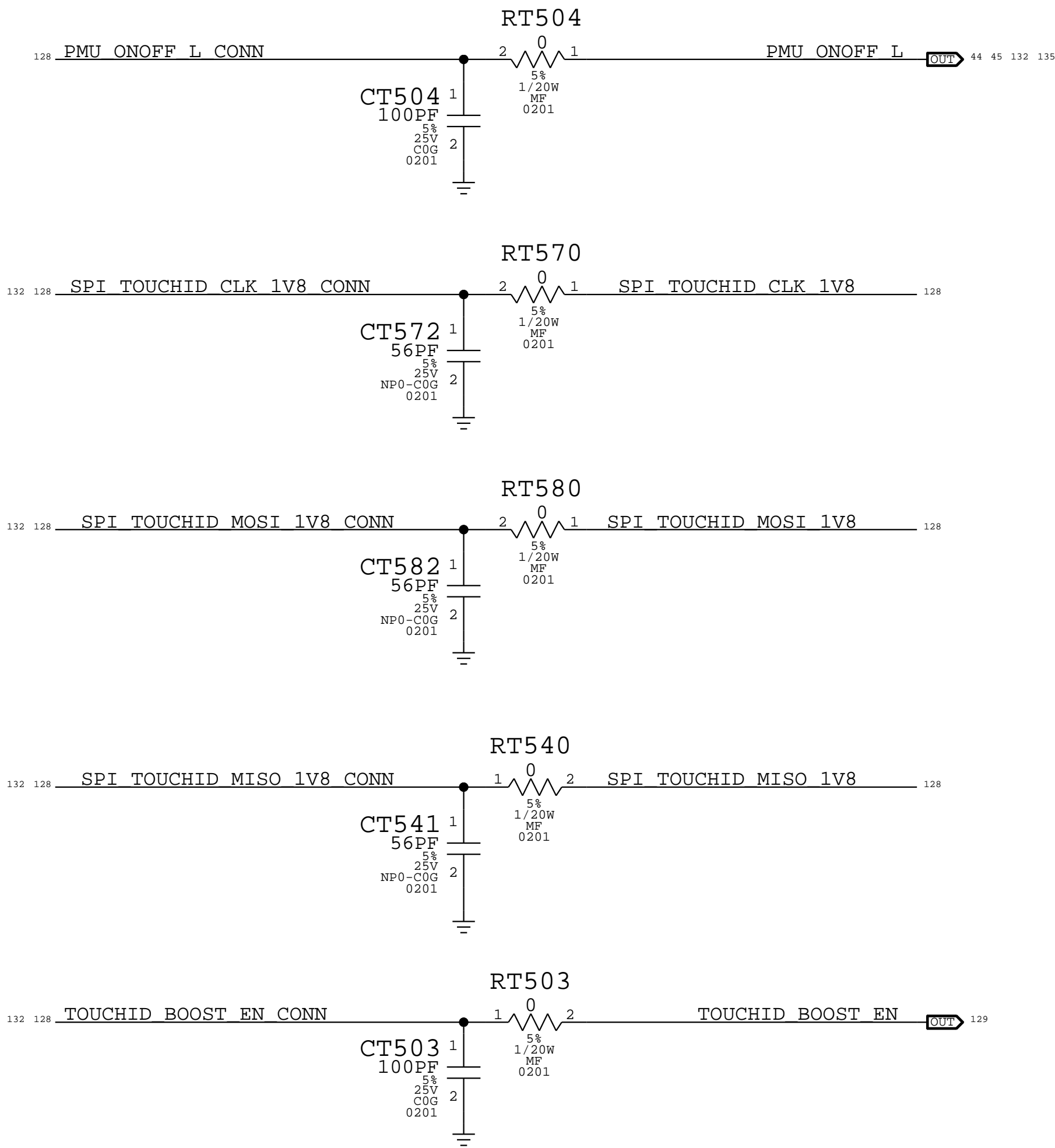


PAGE TITLE		
TRACKPAD CONNECTOR		
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	PAGE	254 OF 998
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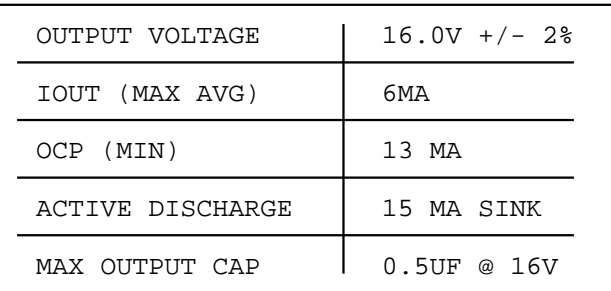
ISOLATE FROM OTHER COMPONENTS / NETS AS MUCH AS POSSIBLE



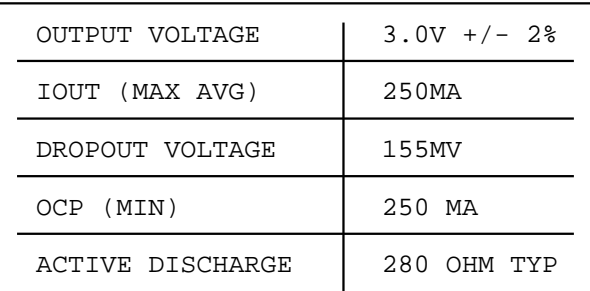
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	REVISION	2.0.0
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	PAGE	255 OF 998
	SHEET	128 OF 156

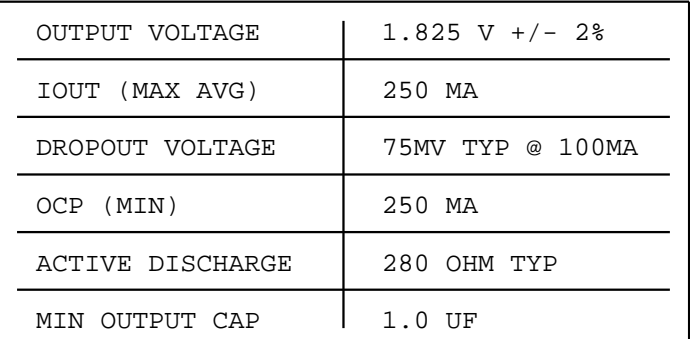
EMC FILTER



EMC FILTER



EMC FILTER



132 128


TOUCHID INT 1V8 CONN

CT650 100PF 1 2 25V C50 0201

RT650 665 1 2 1/20W MF 201

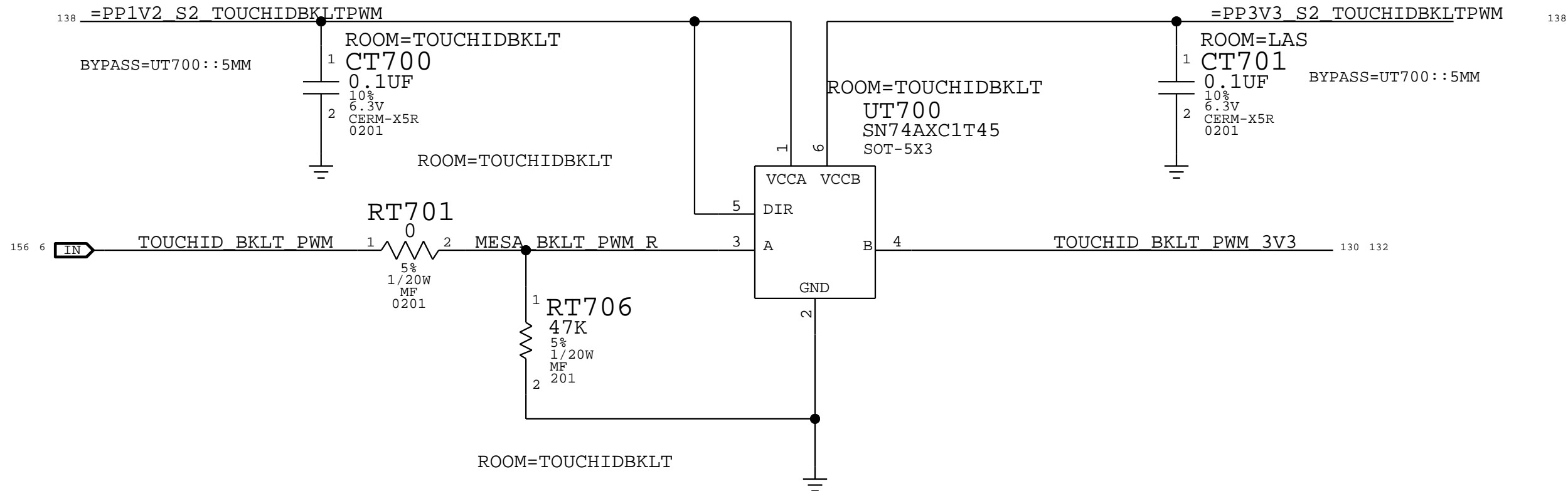
RT651 1.33K 1 2 1/20W MF 201

TOUCHID INT

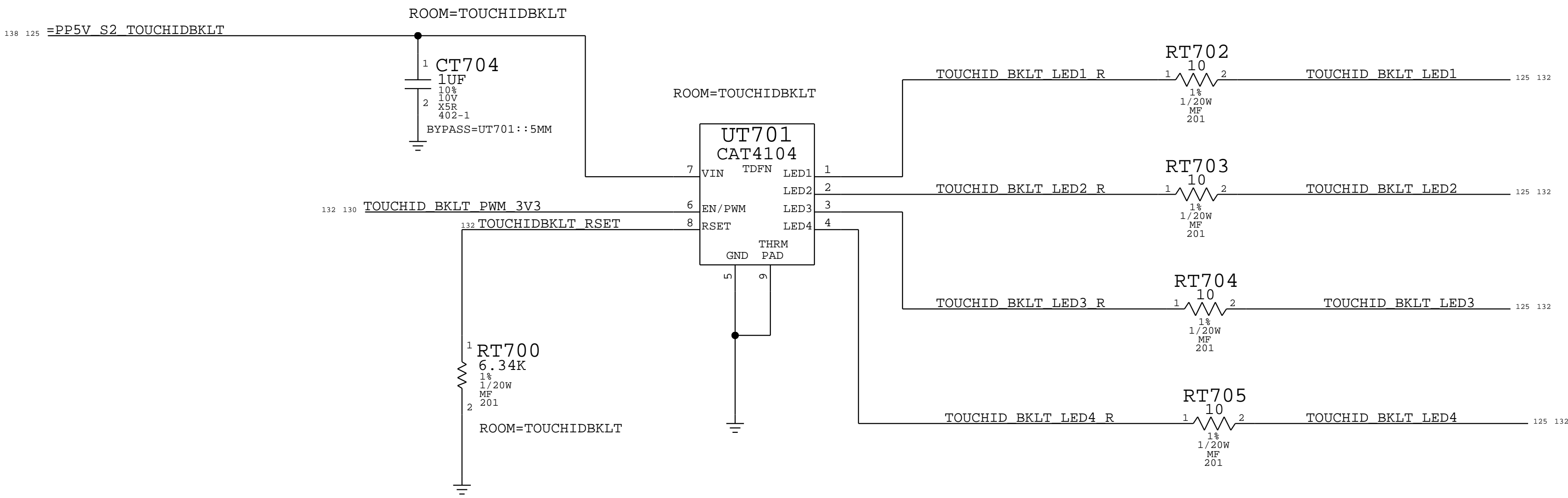
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 Apple Inc.	DRAWING NUMBER	SIZE	
	051-06558	D	
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	BRANCH		
	PAGE	256 OF 998	
	SHEET	129 OF 156	

*** OK2INTEGRATE ***

TOUCHID BKLT PWM LEVEL SHIFTER



TOUCHID BKLT LED DRIVER



CURRENT PER RAIL

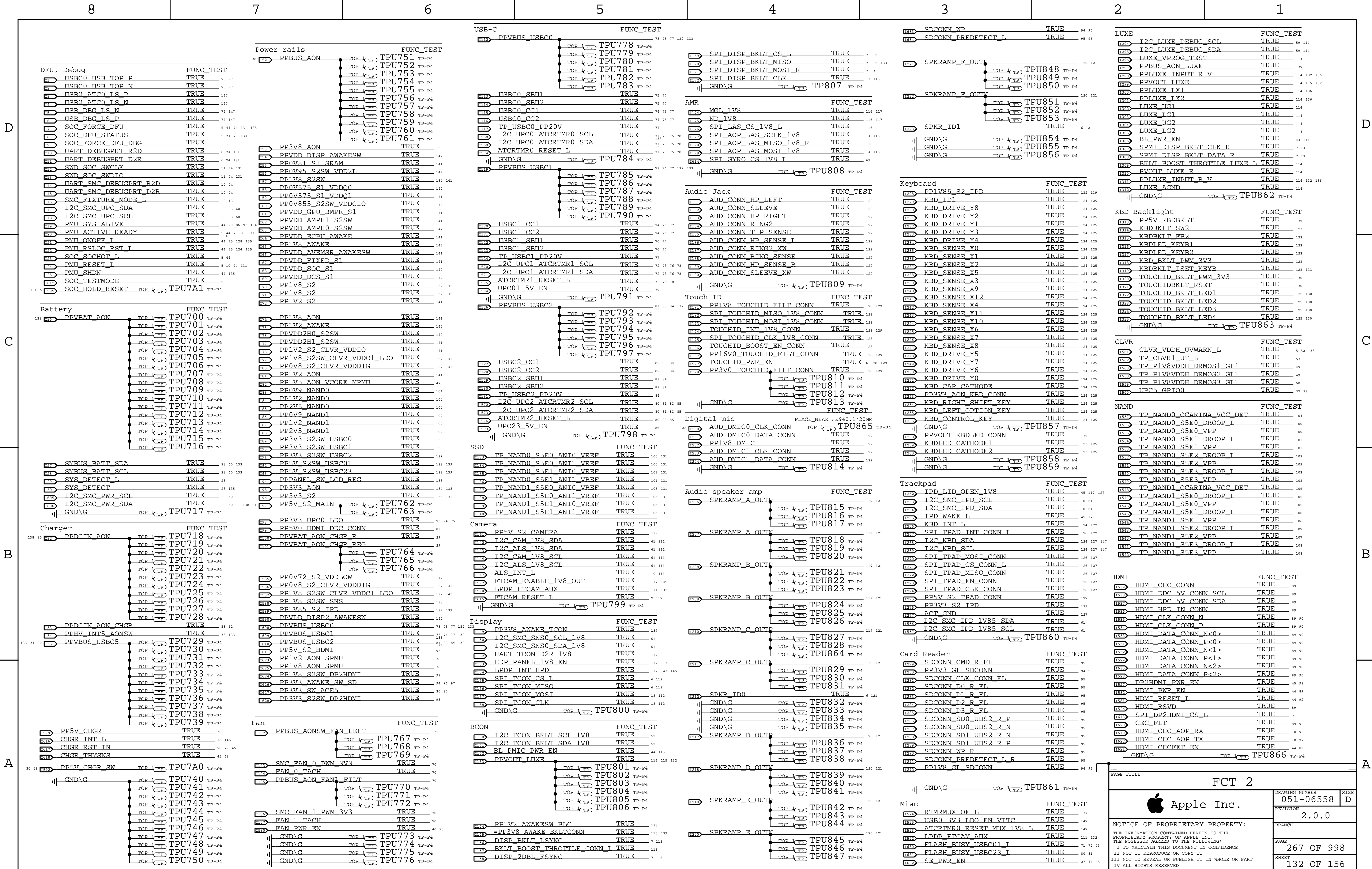
RAIL	TYPICAL	PEAK
1.2 S2	10UA	1.2MA
3 AON	10UA	8 MA
5V S2	80MA	80 MA

4X LEDS, 20MA EACH LED

PAGE TITLE		
TOUCHID_BACKLIGHT		
	DRAWING NUMBER	051-06558
	REVISION	2.0.0
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	PAGE	257 OF 998
	SHEET	130 OF 156

BOM_COST_GROUP=SOC

	8	7	6	5	4	3	2	1	
	NANDO TEST POINTS		NAND1 TEST POINTS		SOC MISC DEBUG TEST-POINTS		TEST POINTS REQUESTED BY AUDIO TEAM		
D	104 103 102 101 100	NANDO LPB L	TPU603	TP-P4	109 108 107 106 105	NAND1 LPB L	TPU636	TP-P4	
	107 106 105 103 102 101 100 8	NAND BFH	TPU604	TP-P4	108 107 106 105	NAND1 BOOT2	TPU637	TP-P4	
	103 102 101 100	NANDO BOOT2	TPU605	TP-P4	105	NAND1 S5E0 SWD UID0	TPU638	TP-P4	
	100	NANDO S5E0 SWD UID0	TPU606	TP-P4	106	NAND1 S5E1 SWD UID0	TPU639	TP-P4	
	101	NANDO S5E1 SWD UID0	TPU607	TP-P4	107	NAND1 S5E2 SWD UID0	TPU640	TP-P4	
	102	NANDO S5E2 SWD UID0	TPU608	TP-P4	108	NAND1 S5E3 SWD UID0	TPU641	TP-P4	
	103	NANDO S5E3 SWD UID0	TPU609	TP-P4	105	NAND1 S5E0 SWD UID1	TPU642	TP-P4	
	100	NANDO S5E0 SWD UID1	TPU610	TP-P4	106	NAND1 S5E1 SWD UID1	TPU643	TP-P4	
	101	NANDO S5E1 SWD UID1	TPU611	TP-P4	107	NAND1 S5E2 SWD UID1	TPU644	TP-P4	
	102	NANDO S5E2 SWD UID1	TPU612	TP-P4	108	NAND1 S5E3 SWD UID1	TPU645	TP-P4	
C	103	NANDO S5E3 SWD UID1	TPU613	TP-P4	109 108 107 106 105	NAND1 PFN L	TPU646	TP-P4	
	104 103 102 101 100	NANDO PFN L	TPU614	TP-P4	108 107 106 105 8	NAND1 PCIE RESET L	TPU647	TP-P4	
	103 102 101 100 8	NANDO PCIE RESET L	TPU615	TP-P4	11	SWD NAND1 SWDIO	TPU648	TP-P4	
	11	SWD NAND0 SWDIO	TPU616	TP-P4	11	SWD NAND1 SWCLK	TPU649	TP-P4	
	11	SWD NAND0 SWCLK	TPU617	TP-P4	108 107 106 105	NAND1 WP L	TPU650	TP-P4	
	103 102 101 100	NANDO WP L	TPU618	TP-P4	110 8	NAND1 CLKREQ0 L	TPU651	TP-P4	
	110 8	NANDO CLKREQ0 L	TPU619	TP-P4	110 8	NAND1 CLKREQ1 L	TPU652	TP-P4	
	110 8	NANDO CLKREQ1 L	TPU620	TP-P4	110 8	NAND1 CLKREQ2 L	TPU653	TP-P4	
	110 8	NANDO CLKREQ2 L	TPU621	TP-P4	110 8	NAND1 CLKREQ3 L	TPU654	TP-P4	
	110 8	NANDO CLKREQ3 L	TPU622	TP-P4	106	NAND1 S5E0 PCIE RESREF	TPU655	TP-P4	
B	100	NANDO S5E0 PCIE RESREF	TPU623	TP-P4	106	NAND1 S5E1 PCIE RESREF	TPU656	TP-P4	
	101	NANDO S5E1 PCIE RESREF	TPU624	TP-P4	107	NAND1 S5E2 PCIE RESREF	TPU657	TP-P4	
	102	NANDO S5E2 PCIE RESREF	TPU625	TP-P4	108	NAND1 S5E3 PCIE RESREF	TPU658	TP-P4	
	103	NANDO S5E3 PCIE RESREF	TPU626	TP-P4	109 108 107 106 105	NAND1 RESET L	TPU659	TP-P4	
	104 103 102 101 100	NANDO RESET L	TPU627	TP-P4	106	NAND1 S5E0 ZQ 0	TPU660	TP-P4	
	100	NANDO S5E0 ZQ 0	TPU628	TP-P4	105	NAND1 S5E0 ZQ 1	TPU661	TP-P4	
	100	NANDO S5E0 ZQ 1	TPU629	TP-P4	106	NAND1 S5E1 ZQ 0	TPU662	TP-P4	
	101	NANDO S5E1 ZQ 1	TPU630	TP-P4	106	NAND1 S5E1 ZQ 1	TPU663	TP-P4	
	101	NANDO S5E1 ZQ 0	TPU631	TP-P4	107	NAND1 S5E2 ZQ 0	TPU664	TP-P4	
	102	NANDO S5E2 ZQ 0	TPU632	TP-P4	107	NAND1 S5E2 ZQ 1	TPU665	TP-P4	
A	102	NANDO S5E2 ZQ 1	TPU633	TP-P4	108	NAND1 S5E3 ZQ 1	TPU666	TP-P4	
	103	NANDO S5E3 ZQ 1	TPU634	TP-P4	108	NAND1 S5E3 ZQ 0	TPU667	TP-P4	
	103	NANDO S5E3 ZQ 0	TPU635	TP-P4	108	NAND1 S5E3 ZQ 0	TPU667	TP-P4	
	100	TP NAND0 S5E0 JTAG TDI	TPU668	TP-P4	107 106	NAND1 S5E1 JTAG TDO	TPU680	TP-P4	
	103	TP NAND0 S5E3 JTAG TDO	TPU669	TP-P4	108 107	NAND1 S5E2 JTAG TDO	TPU681	TP-P4	
	103 102 101 100	NANDO JTAG SEL	TPU670	TP-P4	105	TP NAND1 S5E0 JTAG TDI	TPU682	TP-P4	
	103 102 101 100	NANDO JTAG TRST L	TPU671	TP-P4	108	TP NAND1 S5E3 JTAG TDO	TPU683	TP-P4	
	132 100	TP NAND0 S5E0 ANI1 VREF	TPU672	TP-P4	108 107 106 105	NAND1 JTAG SEL	TPU684	TP-P4	
	132 100	TP NAND0 S5E0 ANI0 VREF	TPU673	TP-P4	108 107 106 105	NAND1 JTAG TRST L	TPU685	TP-P4	
	132 101	TP NAND0 S5E1 ANI1 VREF	TPU674	TP-P4	108 107 106 105	NAND1 JTAG TRST L	TPU685	TP-P4	
	132 101	TP NAND0 S5E1 ANI0 VREF	TPU675	TP-P4	132 105	TP NAND1 S5E0 ANI1 VREF	TPU686	TP-P4	
	102	TP NAND0 S5E2 ANI1 VREF	TPU676	TP-P4	132 105	TP NAND1 S5E0 ANI0 VREF	TPU687	TP-P4	
	102	TP NAND0 S5E2 ANI0 VREF	TPU677	TP-P4	132 106	TP NAND1 S5E1 ANI1 VREF	TPU688	TP-P4	
	103	TP NAND0 S5E3 ANI1 VREF	TPU678	TP-P4	132 106	TP NAND1 S5E1 ANI0 VREF	TPU689	TP-P4	
	103	TP NAND0 S5E3 ANI0 VREF	TPU679	TP-P4	107	TP NAND1 S5E2 ANI1 VREF	TPU690	TP-P4	
	104	TP NAND0 OCARINA VEN2	TPU600	TP-P4	107	TP NAND1 S5E2 ANI0 VREF	TPU691	TP-P4	
				108	TP NAND1 S5E3 ANI1 VREF	TPU692	TP-P4		
				108	TP NAND1 S5E3 ANI0 VREF	TPU693	TP-P4		
				109	TP NAND1 OCARINA VEN2	TPU601	TP-P4		
	FAN TEST POINTS		BSB THERMAL TESTPOINTS		SOC JTAG TEST-POINTS		SOC DEBUG TEST-POINTS		
	70	TP I2C FAN0 SCL	TPU6200	TP-P4	71	ATCR1MR0 THERM D P	TPU6300	TP-P4	
	70	TP I2C FAN0 SDA	TPU6201	TP-P4	71	ATCR1MR0 THERM D N	TPU6301	TP-P4	
	70	TP I2C FAN1 SCL	TPU6202	TP-P4	72	ATCR1MR1 THERM D P	TPU6302	TP-P4	
	70	TP I2C FAN1 SDA	TPU203	TP-P4	73	ATCR1MR1 THERM D N	TPU6303	TP-P4	
				80	ATCR1MR2 THERM D P	TPU6304	TP-P4		
				80	ATCR1MR2 THERM D N	TPU6305	TP-P4		
				34	I2C P3V8AON SCL	TPV001	TP-P5		
				34	I2C P3V8AON SDA	TPV002	TP-P5		
				137 10	SOC DOCK CONNECT	TPU6671	TP-P4		
				113	CODEC_WAKE_L	TRUE	44 118		
	8	7	6	5	4	3	2	1	



SPMU PPS

P3MM	SM	PPU800	1 SPMU BUCK5 LX0	39
P3MM	SM	PPU801	1 SPMU BUCK5 LX1	39
P3MM	SM	PPU802	1 SPMU BUCK5 LX2	39
P3MM	SM	PPU803	1 SPMU BUCK5 LX3	39
P3MM	SM	PPU804	1 SPMU BUCK5 FB R	39
P3MM	SM	PPU805	1 SPMU BUCK5 FB	39
P3MM	SM	PPU806	1 SPMU BUCK6 LX0	39
P3MM	SM	PPU807	1 SPMU BUCK6 FB R	39
P3MM	SM	PPU808	1 SPMU BUCK6 FB	39
P3MM	SM	PPU809	1 SPMU BUCK7 LX0	39
P3MM	SM	PPU810	1 SPMU BUCK7 LX1	39
P3MM	SM	PPU811	1 SPMU BUCK7 LX2	39
P3MM	SM	PPU812	1 SPMU BUCK8 LX0	39
P3MM	SM	PPU813	1 SPMU BUCK8 FB R	39
P3MM	SM	PPU814	1 SPMU BUCK8 FB	39
P3MM	SM	PPU815	1 SPMU BUCK9 LX0	39
P3MM	SM	PPU816	1 SPMU BUCK9 FB R	39
P3MM	SM	PPU817	1 SPMU BUCK9 FB	39
P3MM	SM	PPU818	1 SPMU BUCK10 LX0	39
P3MM	SM	PPU819	1 SPMU BUCK10 LX1	39
P3MM	SM	PPU820	1 SPMU BUCK10 LX2	39
P3MM	SM	PPU821	1 SPMU BUCK10 FB R	39
P3MM	SM	PPU822	1 SPMU BUCK10 FB	39
P3MM	SM	PPU823	1 SPMU BUCK0 LX0	39
P3MM	SM	PPU824	1 SPMU BUCK0 LX1	39
P3MM	SM	PPU825	1 SPMU BUCK0 LX2	39
P3MM	SM	PPU826	1 SPMU BUCK0 LX3	39
P3MM	SM	PPU827	1 SPMU BUCK0 FB	39
P3MM	SM	PPU828	1 SPMU BUCK0 FB R	39
P3MM	SM	PPU829	1 SPMU BUCK1 LX0	39
P3MM	SM	PPU830	1 SPMU BUCK1 LX1	39
P3MM	SM	PPU8031	1 SPMU BUCK1 FB	39
P3MM	SM	PPU832	1 SPMU BUCK1 FB R	39
P3MM	SM	PPU833	1 SPMU BUCK2 LX0	39
P3MM	SM	PPU834	1 SPMU BUCK2 FB	39
P3MM	SM	PPU835	1 SPMU BUCK2 FB R	39
P3MM	SM	PPU836	1 SPMU BUCK3 LX0	39
P3MM	SM	PPU837	1 SPMU BUCK3 FB	39
P3MM	SM	PPU838	1 SPMU BUCK3 FB R	39
P3MM	SM	PPU839	1 SPMU BUCK4 LX0	39

[illegible]

Figure 10: VIPER PPs

The figure displays a list of 24 Peripheral Power (PP) entries and a schematic diagram of the PPU blocks connected to the PP1V8 S1 CLVR VDDH bus.

Peripheral Power (PP) Entries:

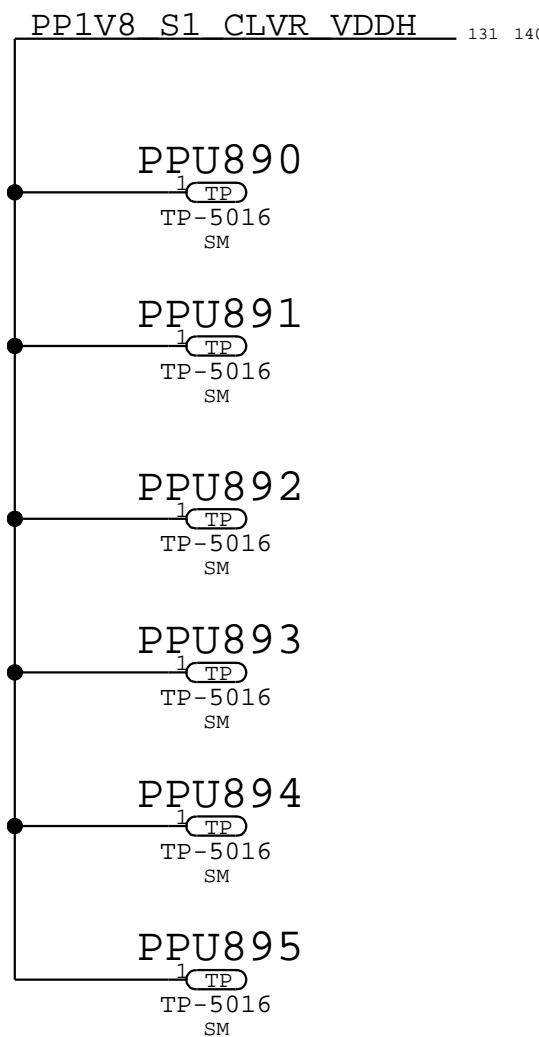
- P3MM_{SM} (PP)¹ MPMU_BUCK0_LX2
- PPU871
- P3MM_{SM} (PP)¹ MPMU_BUCK0_LX3
- PPU872
- P3MM_{SM} (PP)¹ MPMU_BUCK0_FB
- PPU873
- P3MM_{SM} (PP)¹ MPMU_BUCK0_FB_R
- PPU874
- P3MM_{SM} (PP)¹ MPMU_BUCK1_LX0
- PPU875
- P3MM_{SM} (PP)¹ MPMU_BUCK1_LX1
- PPU876
- P3MM_{SM} (PP)¹ MPMU_BUCK1_FB
- PPU877
- P3MM_{SM} (PP)¹ MPMU_BUCK1_FB_R
- PPU878
- P3MM_{SM} (PP)¹ MPMU_BUCK2_LX0
- PPU879
- P3MM_{SM} (PP)¹ MPMU_BUCK2_FB
- PPU880
- P3MM_{SM} (PP)¹ MPMU_BUCK2_FB_R
- PPU881
- P3MM_{SM} (PP)¹ MPMU_BUCK3_LX0
- PPU882
- P3MM_{SM} (PP)¹ MPMU_BUCK3_FB
- PP8
- P3MM_{SM} (PP)¹ MPMU_BUCK3_FB_R
- PPU884
- P3MM_{SM} (PP)¹ MPMU_BUCK4_LX0
- PPU885
- P3MM_{SM} (PP)¹ MPMU_BUCK4_LX1
- PPU886
- P3MM_{SM} (PP)¹ MPMU_BUCK4_LX2
- PPU887
- P3MM_{SM} (PP)¹ MPMU_BUCK4_LX3
- PPU888
- P3MM_{SM} (PP)¹ MPMU_BUCK4_FB
- PPU889
- P3MM_{SM} (PP)¹ MPMU_BUCK4_FB_R

Schematic Diagram:

The diagram shows a vertical bus labeled PP1V8 S1 CLVR VDDH (pins 131, 140). Six PPU blocks are connected to this bus:

- PPU890 (TP-5016 SN)
- PPU891 (TP-5016 SN)
- PPU892 (TP-5016 SN)
- PPU893 (TP-5016 SN)
- PPU894 (TP-5016 SN)
- PPU895 (TP-5016 SN)

VIPER PPS



```

1150  _____ UPC PMU RESET 1V2 _____ TRUE 44 45
                                     TPU6800
137 135 83 76 75 45 _____ UPC PMU RESET 3V3 _____ 1 A
                                     PLACE_SIDE=BOTTOM TP-P5
1150  _____ EDP BKLT 1V29 EN _____ TRUE 45 113
1150  _____ IPD PWR EN _____ TRUE 45 126
1150  _____ IPD PWR EN PMU _____ TRUE 45

PPU8A0
P3MM _____ 1 _____ MPMU VPP OTP _____ 44
SM (PP)

PPU8A3
P3MM _____ 1 _____ SPMU BUCK7 FB _____ 39
SM (PP)

PPU8A5
P3MM _____ 1 _____ SPMU VPP OTP _____ 40
SM (PP)

PPU8A8
P3MM _____ 1 _____ CLVR VDDH UVWARN L _____ 5 52 132
SM (PP)

PPU8A9
P3MM _____ 1 _____ P1V8VDDH ILIMIT THROTTLE L _____
SM (PP)

PPU8B0
P3MM _____ 1 _____ P1V8VDDH PWR EN _____ 44 45 48
SM (PP)

PPU8B1
P3MM _____ 1 _____ P1V8VDDH SLP L _____ 44 48 134
SM (PP)

PP8C0
P3MM _____ 1 _____ P1V8VDDH TLIMIT THROTTLE L _____
SM (PP)

PPU8B2
P3MM _____ 1 _____ P3V8AON LPM _____ 34 44 45
SM (PP)

PPU8B7
P3MM _____ 1 _____ PMU UVWARN L _____ 5 11
SM (PP)

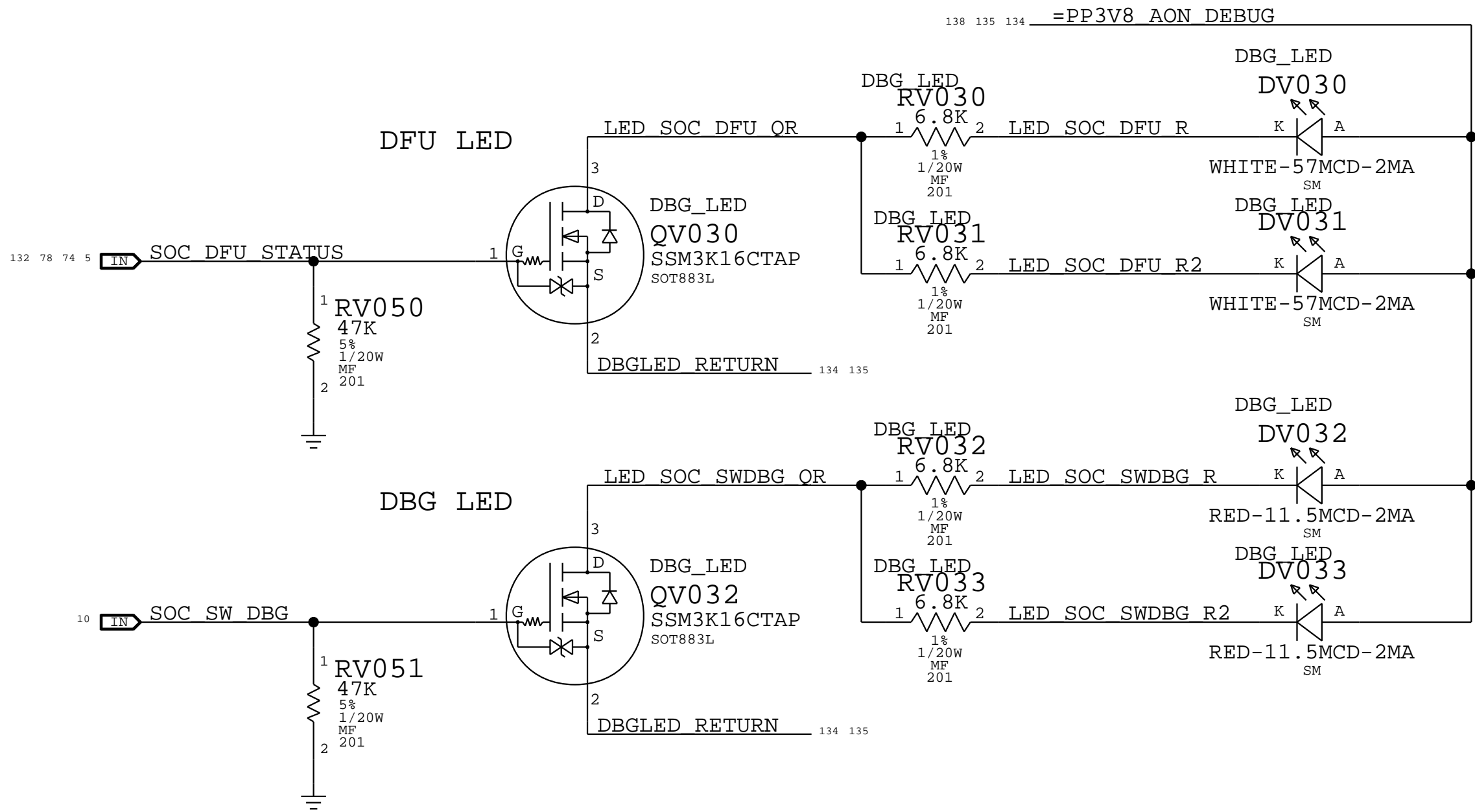
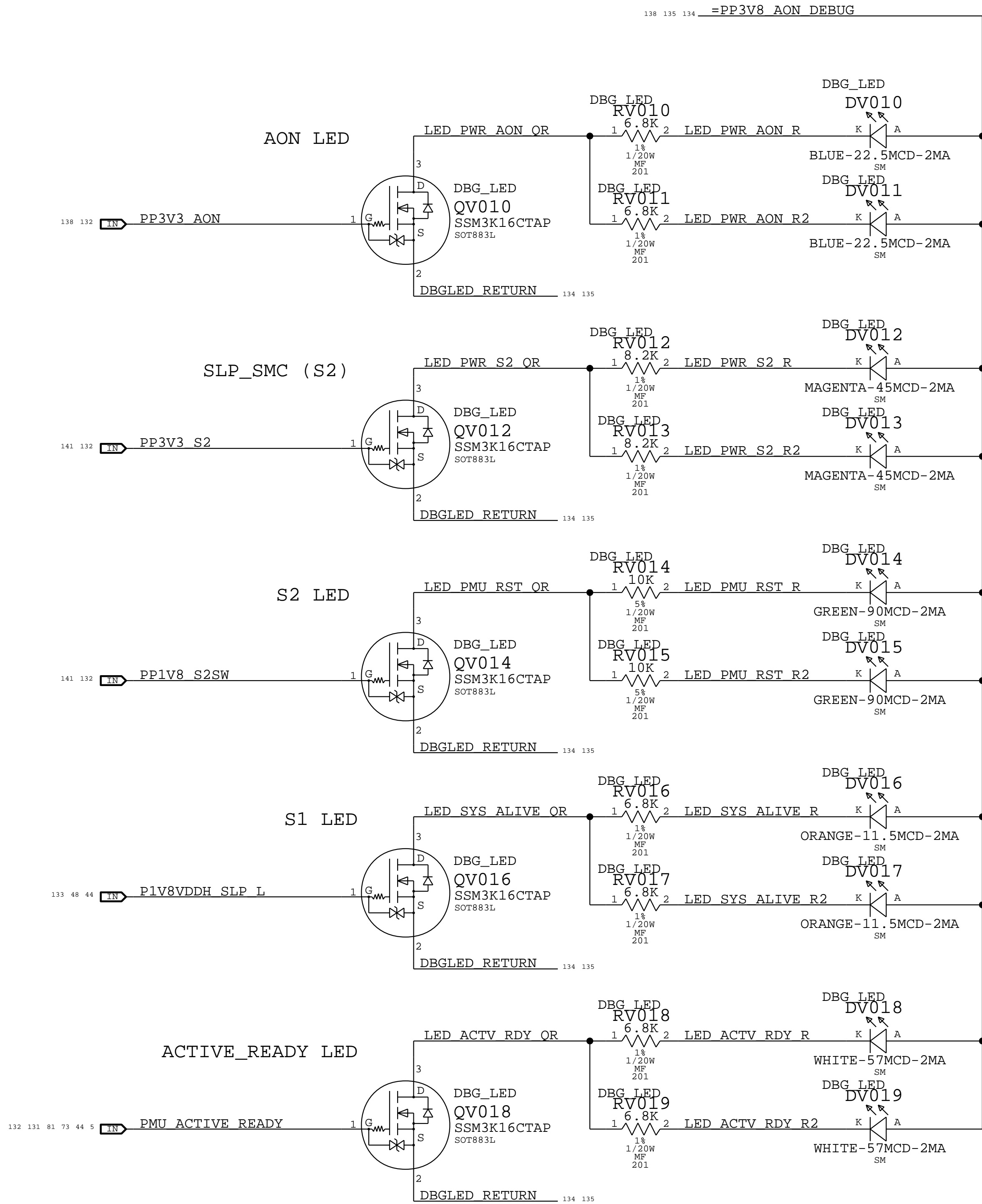
10 TP AON_SLEEP1 RES
MAKE_BASB=TRUE


```

[illegible]

NAND (cont.)		FUNC_TEST	
PPU8C0	12C_SMC_NAND_SCL	TRUE	10 60
PPU8C1	I2C_SMC_NAND_SDA	TRUE	10 60
PPU8C2	NAND0_OCARINA_VREF	TRUE	104
PPU8C3	NAND1_OCARINA_VREF	TRUE	109
PPU8C4	NAND1_S5E0_JTAG_TDO	TRUE	105 106
PPU8C5	P2V5_NAND0_PG00D	TRUE	104
PPU8C6	P2V5_NAND1_PG00D	TRUE	109
PPU8C7	PPVDD_LDO_NAND0_OCARINA	TRUE	104
PPU8C8	PPVDD_LDO_NAND1_OCARINA	TRUE	109
PPU8C9			
PPU8D0			
PPU8D1			
SoC		FUNC_TEST	
11E0	SPI_SOCROM_I1V8_CS_L	TRUE	12
11E7	I2C_SEEPROM_SCL	TRUE	6 12
11E6	I2C_SEEPROM_SDA	TRUE	6 12
NAND (cont.)		FUNC_TEST	
11E0	NAND0_OCARINA_TDEV1	TRUE	104
11E0	NAND1_OCARINA_TDEV2	TRUE	109 133
11E0	NAND0_S5E0_JTAG_TDO	TRUE	100 101
11E0	NAND0_S5E1_JTAG_TDO	TRUE	101 102
11E0	NAND0_S5E2_JTAG_TDO	TRUE	102 103
11E0	NAND1_OCARINA_TDEV1	TRUE	109
11E0	NAND1_OCARINA_TDEV2	TRUE	109 133
11E0	P2V5_NAND0_EN_R	TRUE	104
11E0	P2V5_NAND1_EN_R	TRUE	109
PPU8D9		FUNC_TEST	
PMICs		FUNC_TEST	
11E0	PMU_CLK32K_CLKR	TRUE	45 52 53
11E0	PMU_VDDH1	TRUE	42
11E0	SPMI_NIUB_MPMU_CLK	TRUE	13 44
11E0	SPMI_NIUB_MPMU_DATA	TRUE	13 44
11E0	SPMI_NIUB_SPMU_CLK	TRUE	13 40
11E0	SPMI_NIUB_SPMU_DATA	TRUE	13 40
11E0	SWD_NIUB_PMU_SWCLK	TRUE	11 13
11E0	SWD_NIUB_PMU_SWPIO	TRUE	11 13
11E0	PMU_FAULT_OUT_L	TRUE	40 44
11E0	DEBUG_SPMU_GPIO16	TRUE	45
WLBT		FUNC_TEST	
11E0	PMU_CLK32K_WLBT	TRUE	45 98 99
11E0	TPT_WLAN_JTAG_TCK	TRUE	98 99
11E0	TPT_WLAN_JTAG_TDI	TRUE	98
11E0	TPT_WLAN_JTAG_TMS	TRUE	98 99
11E0	TPT_WLAN_JTAG_TRSTN	TRUE	98
11E0	WLBT_RESET_L		
11E0	BT_TIME_SYNC	TRUE	6 98 99
11E0	WLBT_PWR_EN	TRUE	44 45 98
IPD		FUNC_TEST	
11E0	CAPSLOCK_LED_EN	TRUE	124
11E0	IOXP1_RESET_L	TRUE	124
11E0	IOXP2_RESET_L	TRUE	124
11E0	KDBBK1T_ISKT_KEYB	TRUE	123 132
Sensor		FUNC_TEST	
11E0	AIRFLOW_C_THMSNS	TRUE	45 68
11E0	AIRFLOW_L_THMSNS	TRUE	45 68
11E0	AIRFLOW_R_THMSNS	TRUE	45 68
11E0	DCIN_VSENSE	TRUE	44 62
11E0	FINSTACK_L_THMSNS	TRUE	45 68
11E0	FINSTACK_R_THMSNS	TRUE	45 68
11E0	MEMU_THMSNS	TRUE	45 68
11E0	P1V8VDDH_THMSNS_1	TRUE	45 68
11E0	P1V8VDDH_THMSNS_2	TRUE	45 68
11E0	P1V8VDDH_THMSNS_3	TRUE	45 68
11E0	P3V8AON_THMSNS	TRUE	45 68
11E0	PRUS_VSENSE	TRUE	45 62
11E0	SOC_THMSNS_1	TRUE	45 68
11E0	SPMU_THMSNS	TRUE	45 68
11E0	WING_L_THMSNS	TRUE	45 68
11E0	WING_R_THMSNS	TRUE	45 68
11E0	WLBT_THMSNS	TRUE	45 68

Debug LEDs



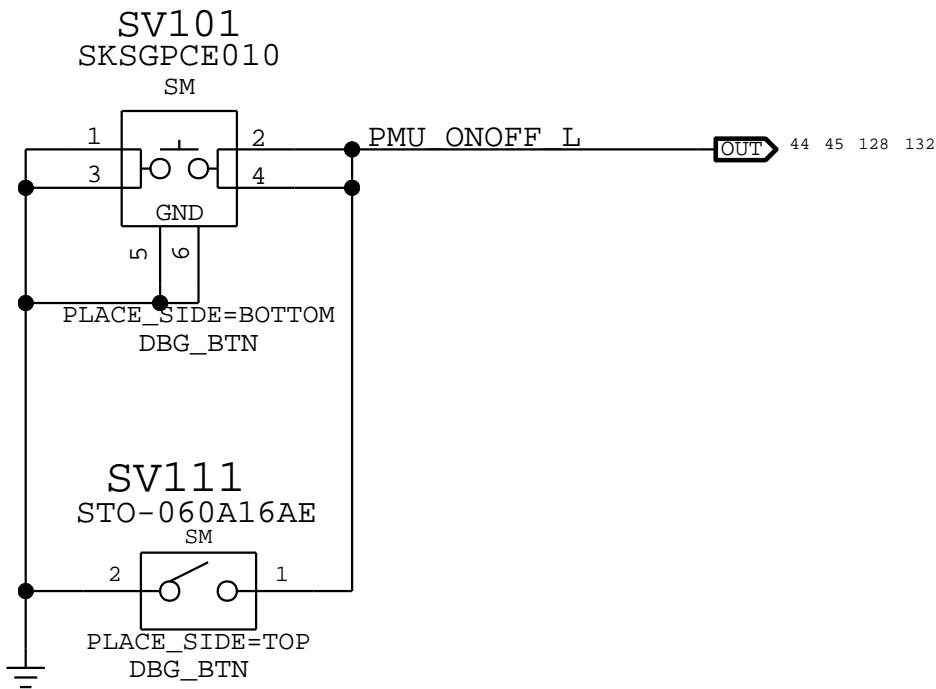
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	REVISION		2.0.0		D
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BOM_COST_GROUP=DEBUG

POWER BUTTON

Imitate a user-facing Power Button press, many functions:

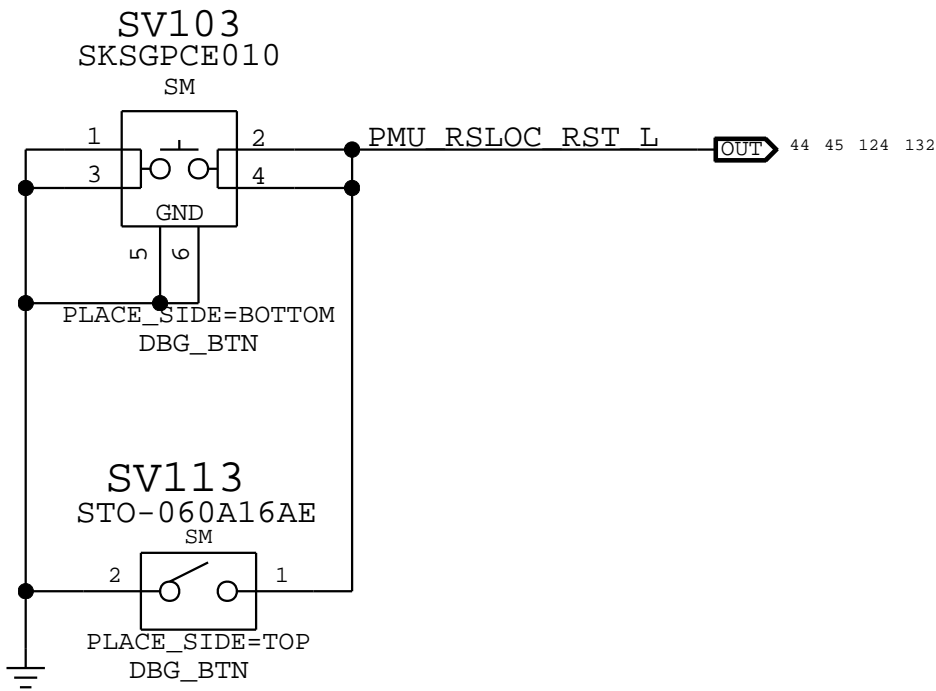
- Press to Wake from any state
- Combine with RSL0C (see RSL0C)
- Hold for 8sec to trigger "one-finger reset"
- - Similar to PMU RESET, except SW gets a warning to initiate panic-flow



RSLOC BUTTON

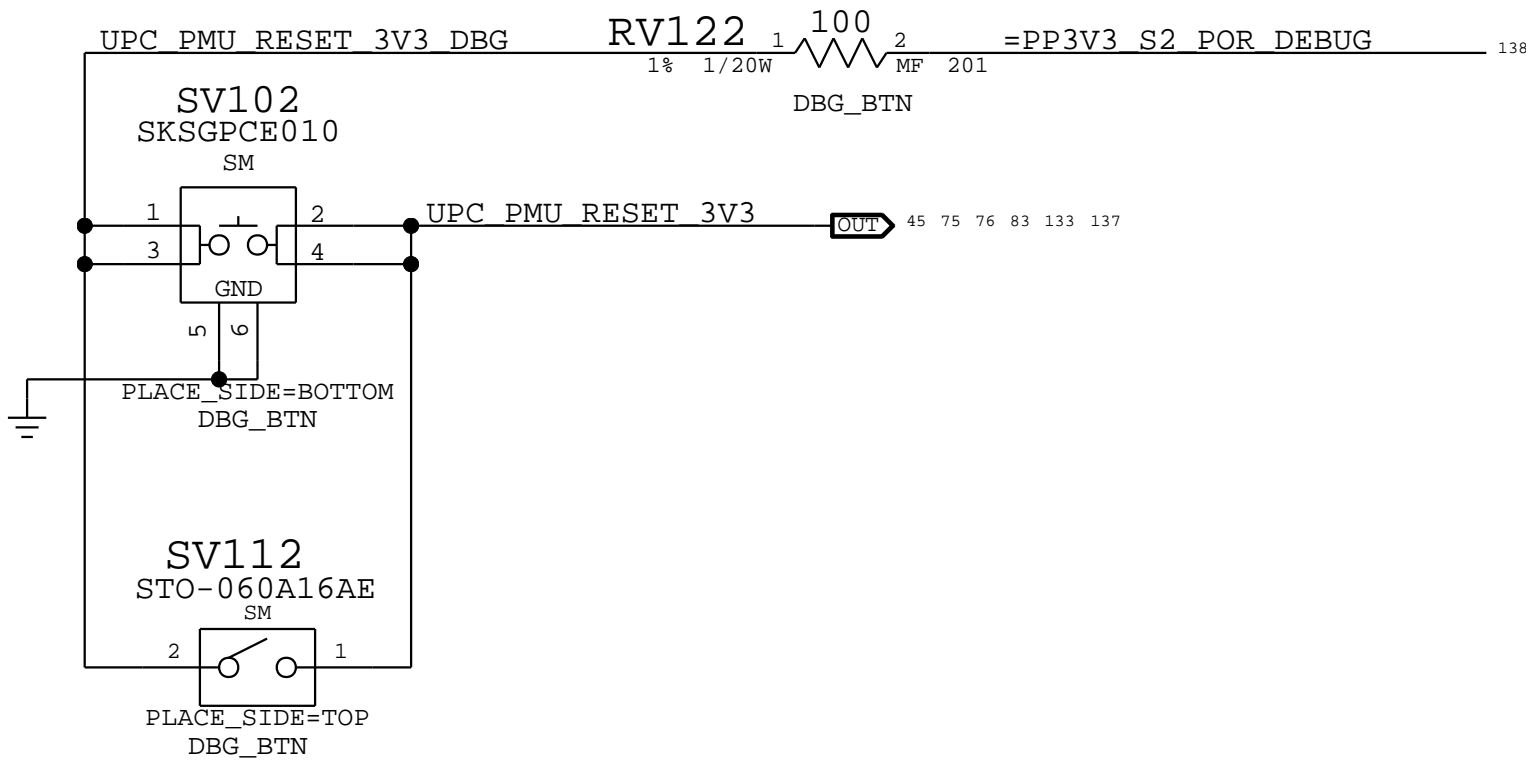
Imitate a user-facing key combo Right-Shift + Left-Option + Control:

- Hold RSLOC 4sec, then press Power Button to initiate PMU RESET
- Hold RSLOC 4sec, then hold Power Button 4sec to power-cycle P3V8AON VR
- Hold Power Button 1sec, then hold RSLOC 10sec to trigger PMU RESET into DFU (continue holding first button when second button is added)



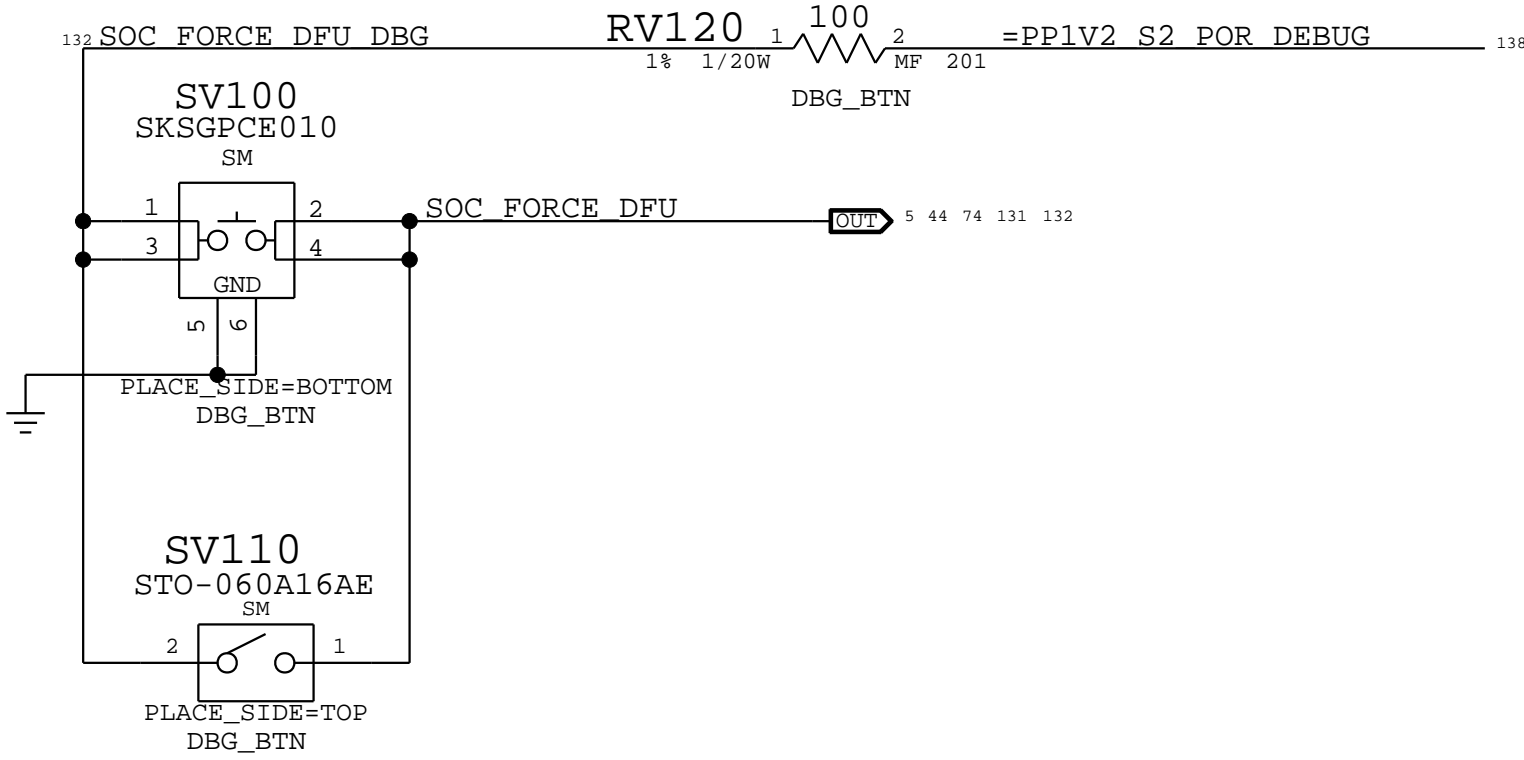
PMU RESET

PMU transitions to OFF and automatically proceeds up to AWAKE



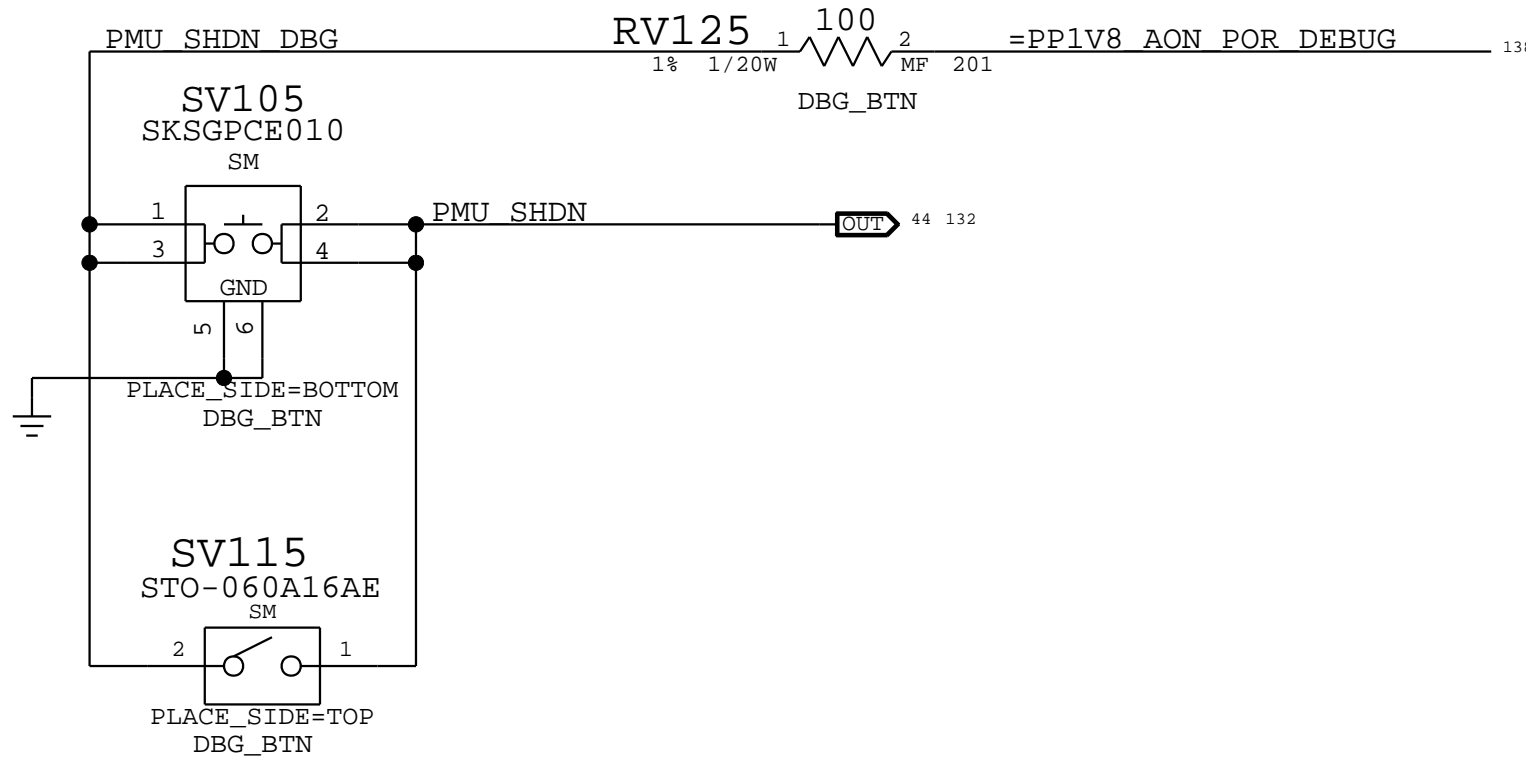
FORCE DFU

Hold during OFF->AWAKE transition to enter SOC's "Debug Firmware Update" mode



PMU SHUTDOWN

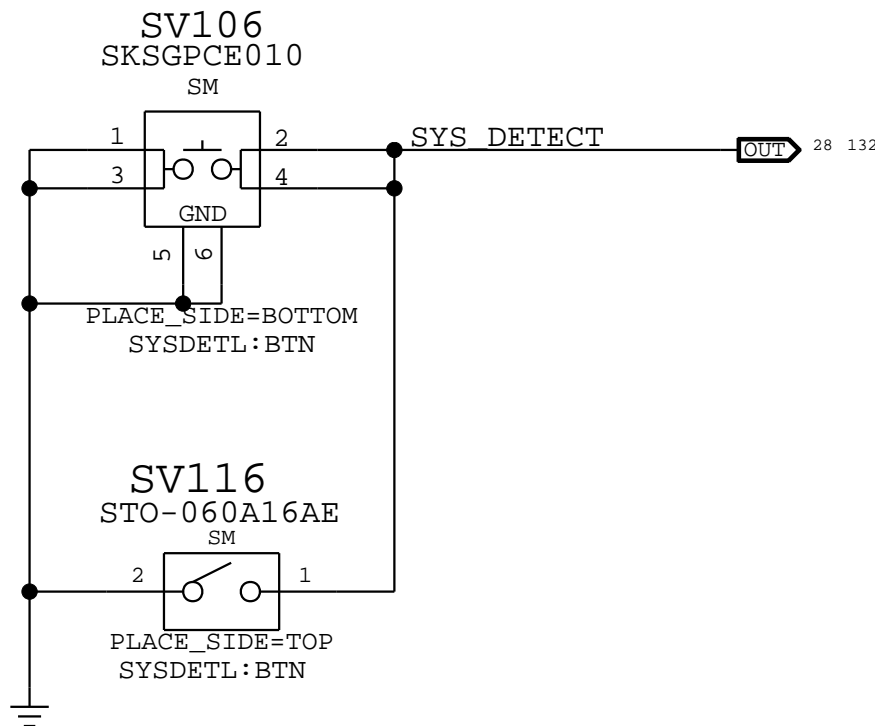
PMU transitions to OFF state and waits for a WAKE source*



SYS_DETECT (Battery Disconnect)

Imitate unplugging the battery signal flex, to disconnect MLB from Battery power

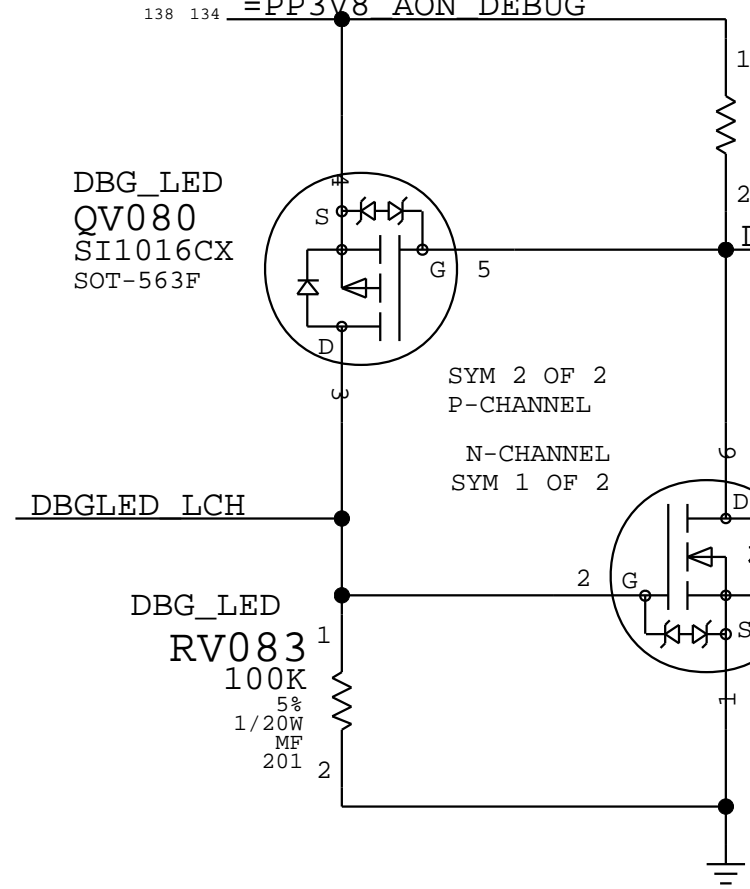
- Disconnect all DCIN sources, then hold SYS_DETECT for 2sec. MLB will completely power down



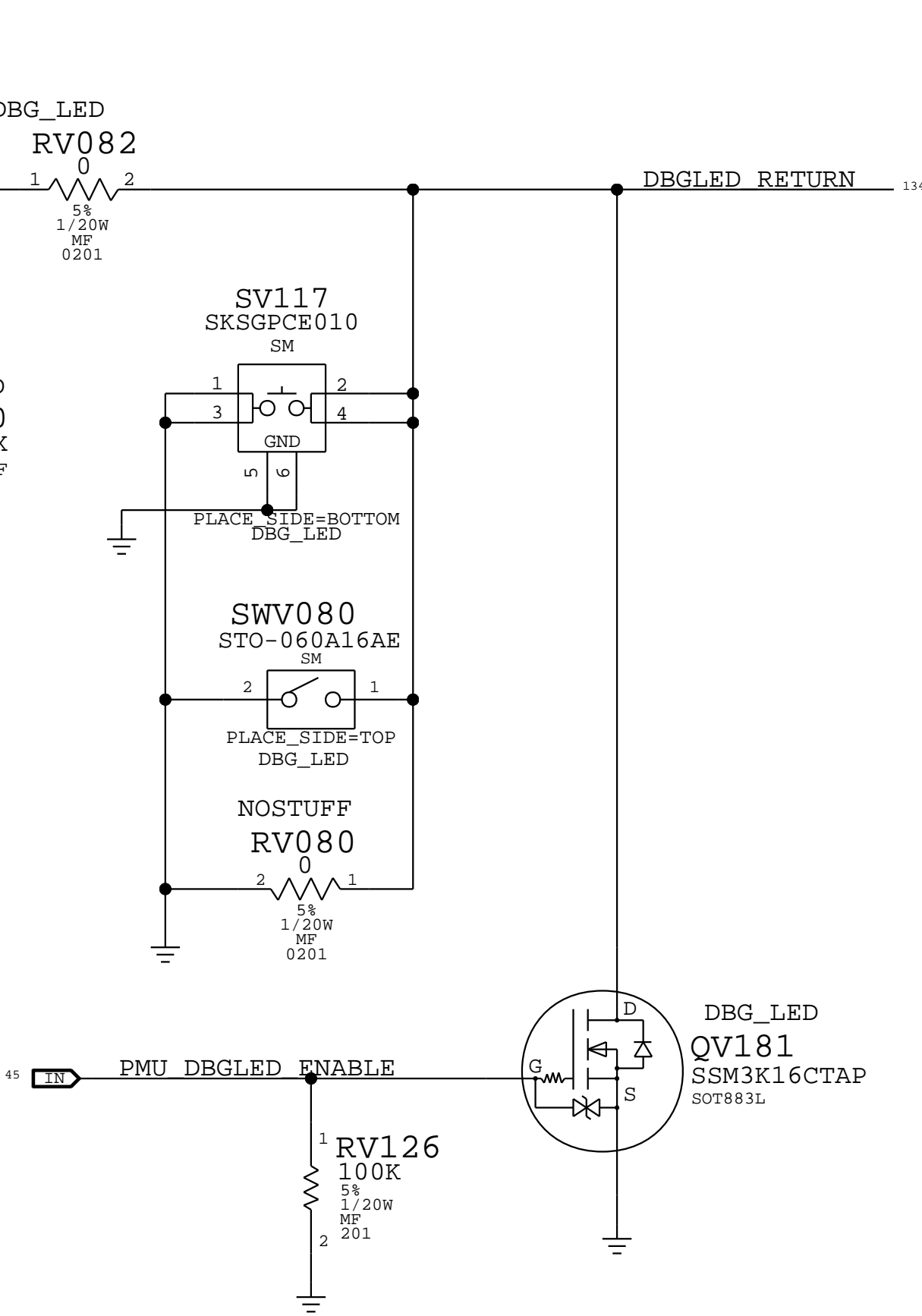
Debug LED Latch

Press button once to engage.

Remove power to disengage.



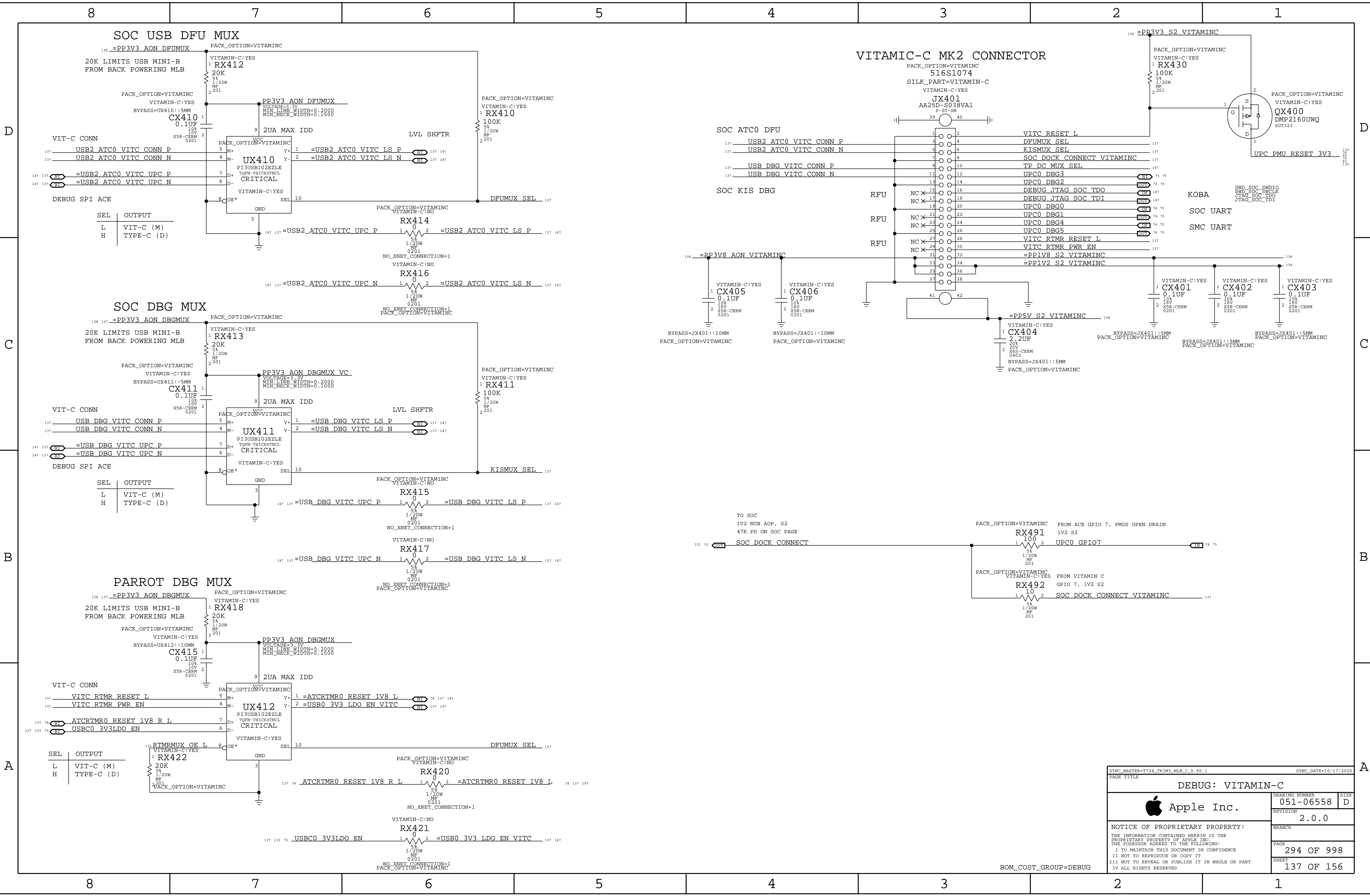
Debug LED Enable




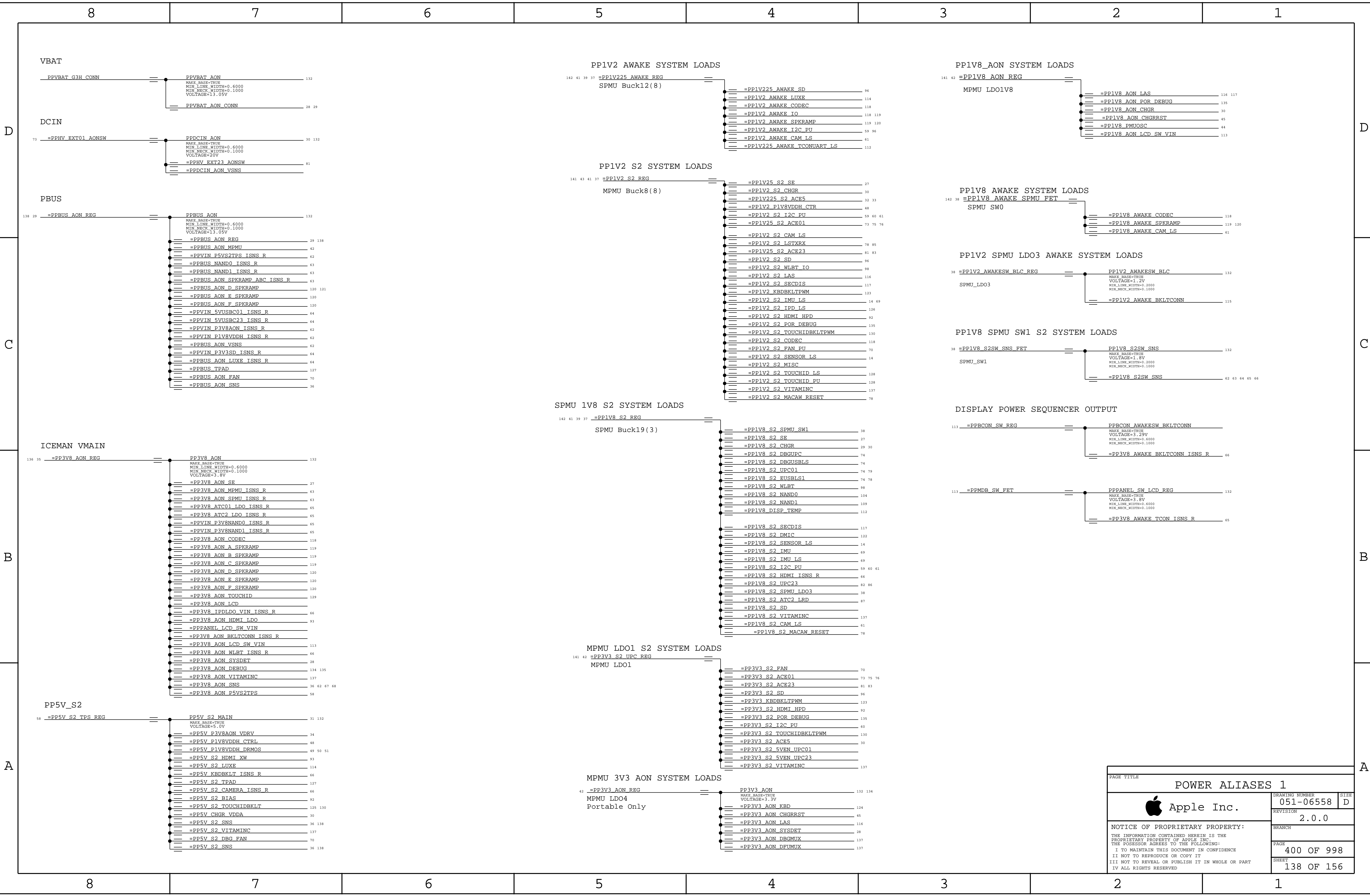
- *WAKE sources in OFF:
- CHGR_AUX_OK (DCIN present)
 - IPD_LID_OPEN_1V8 (Lid is open)
 - PMU_ONOFF_L (User Power Button)


PAGE TITLE		
Debug: Buttons		
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BOM_COST_GROUP=DEBUG



SYNC_MASTER=T724_TKIM3_MLB_C_0.50.1		SYNC_DATE=10/17/2020		
PAGE TITLE				
DEBUG: VITAMIN-C				
 Apple Inc.		DRAWING NUMBER	051-06558	SIZE
		REVISION	2.0.0	D
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POWER ALIASES 1			
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	REVISION	2.0.0	
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		SHEET	138 OF 156

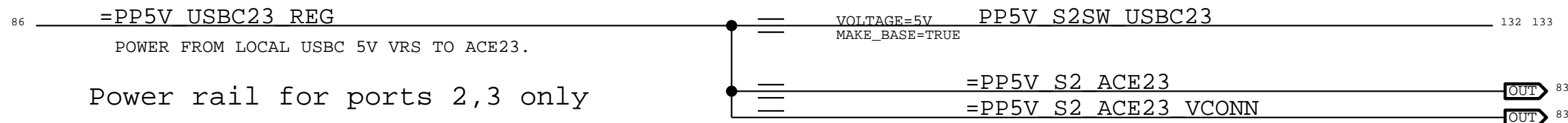
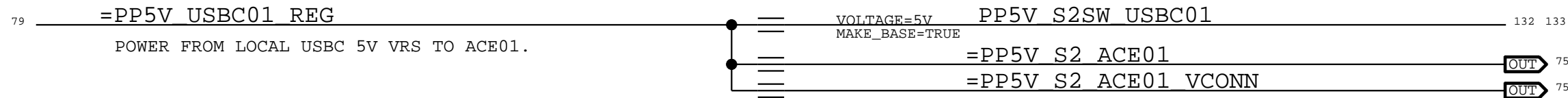
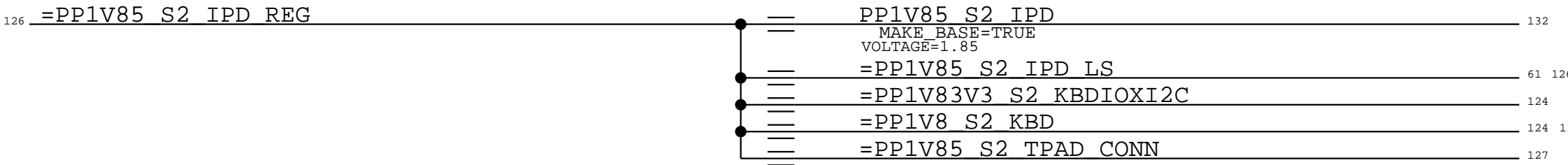
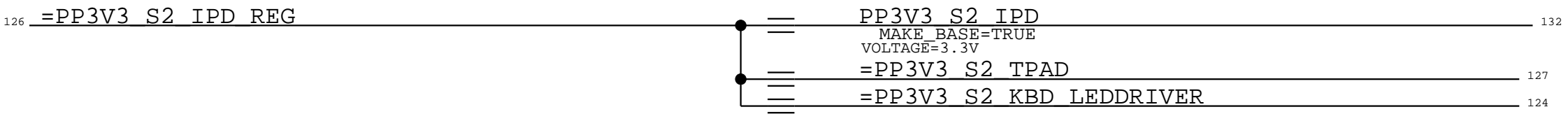
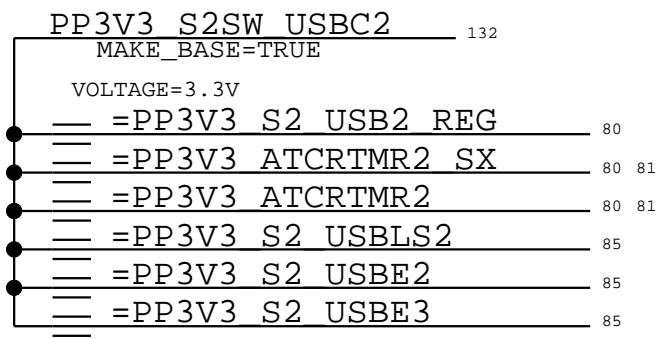
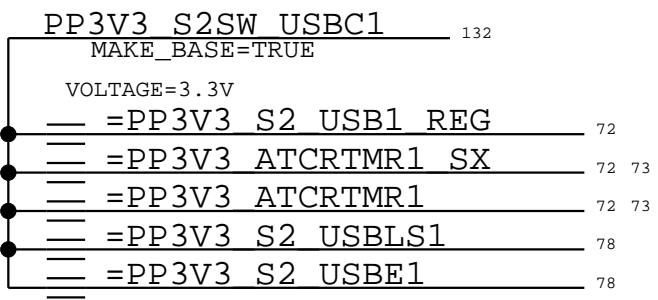
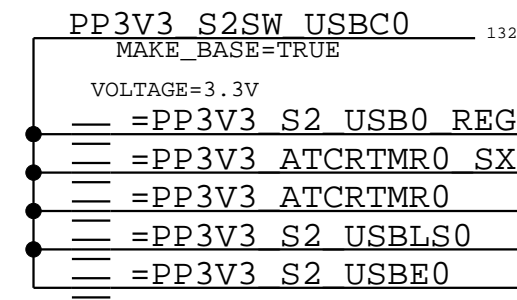
THIS PAGE WILL BE USED FOR SYSTEM / SUBSYSTEM ALIASES

USBC REQUIRED POWER ALIASES

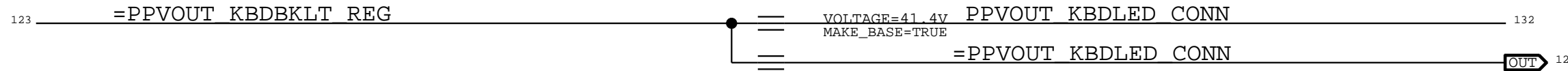
IPD: KEYBOARD / TRACKPAD

PP3V3_S2_IPD (LDO) ALIASES

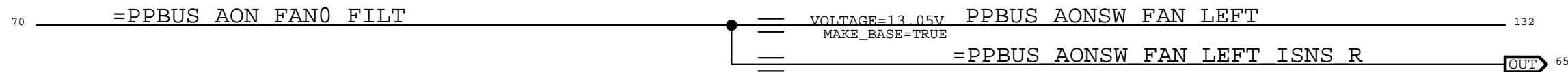
PP1V85_S2_IPD (LDO) ALIASES



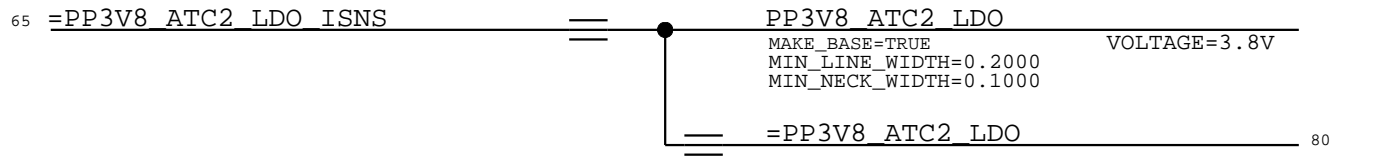
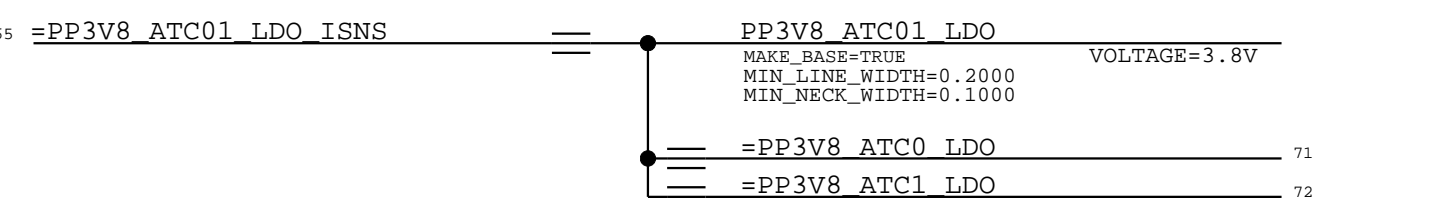
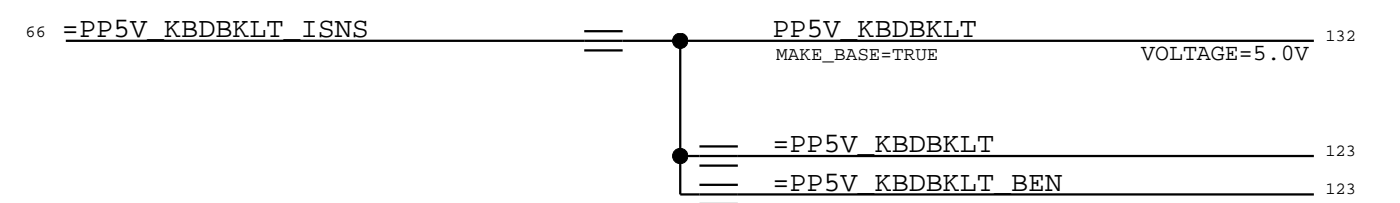
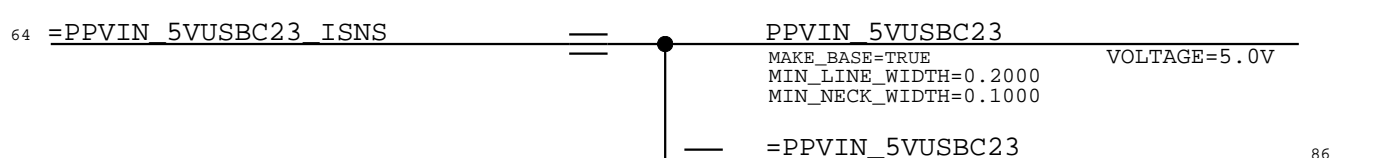
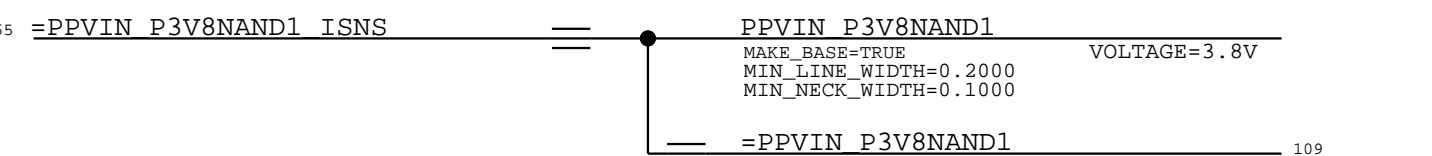
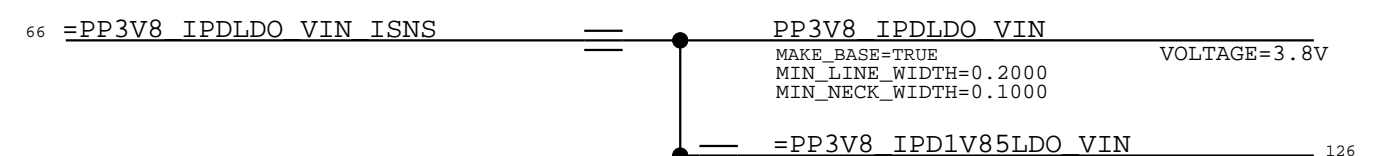
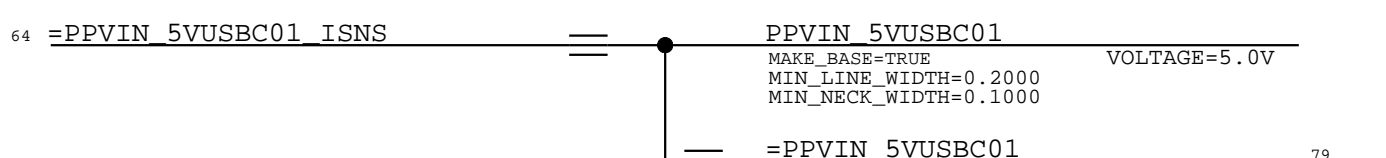
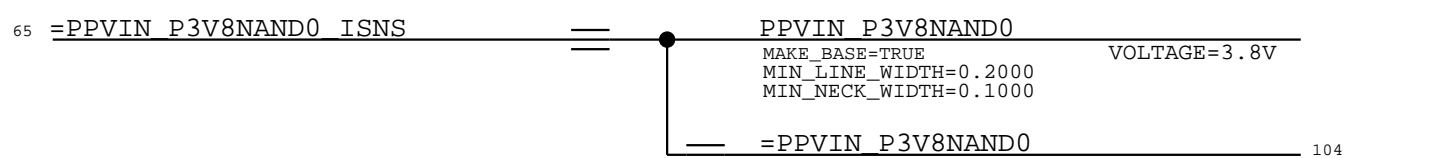
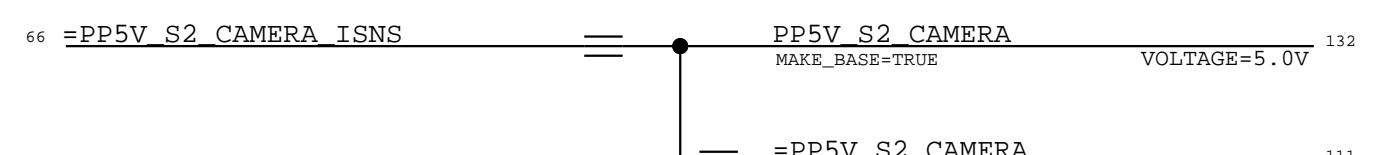
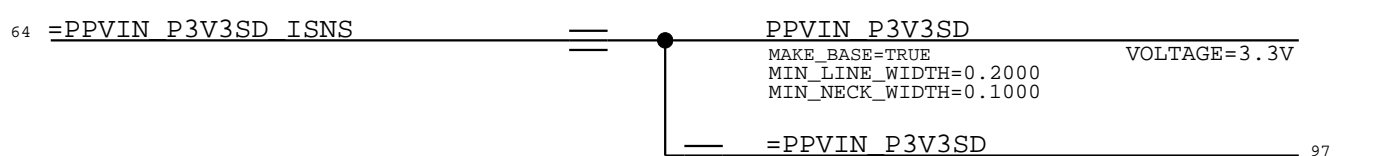
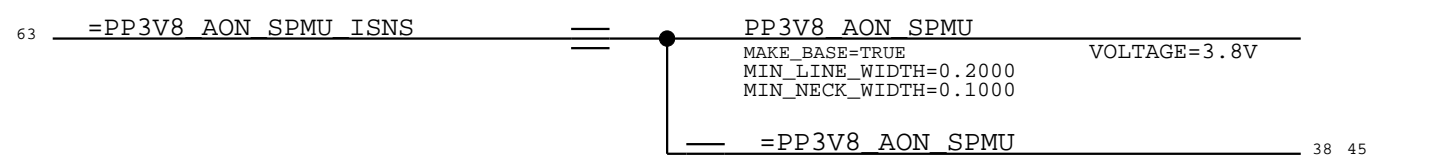
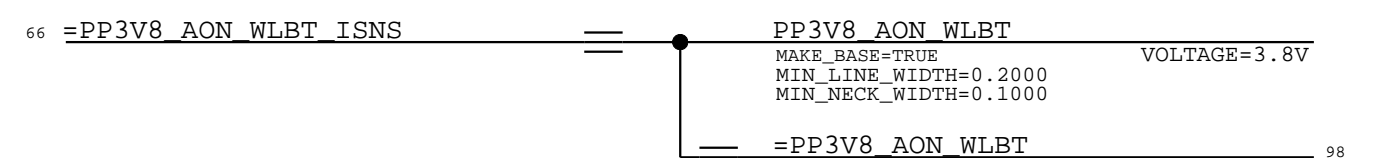
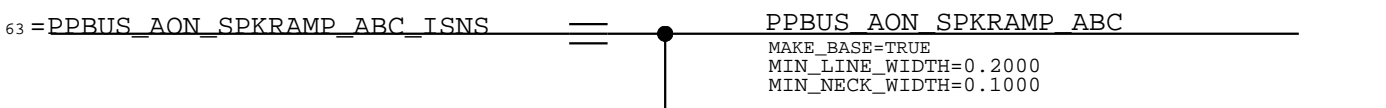
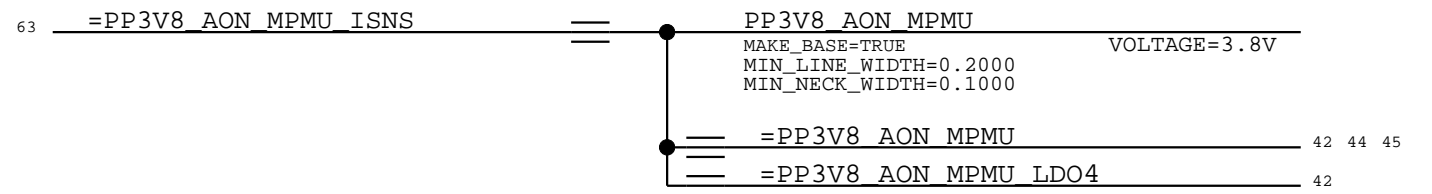
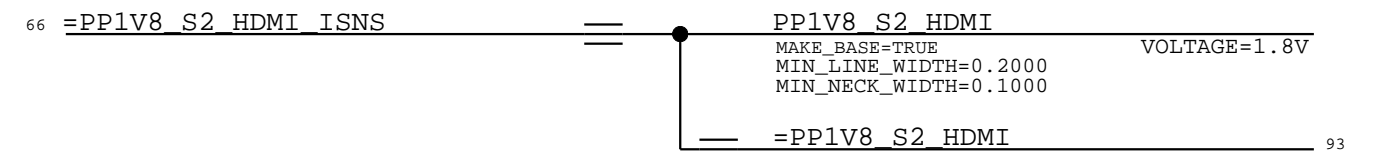
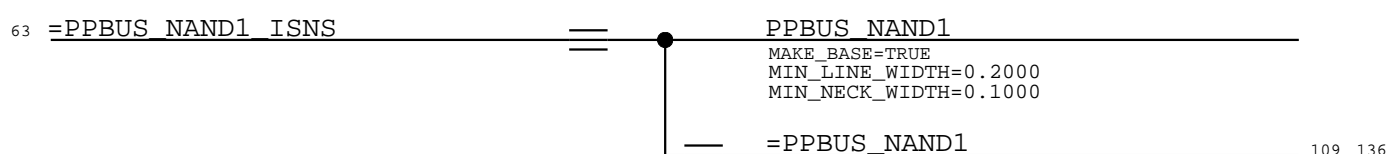
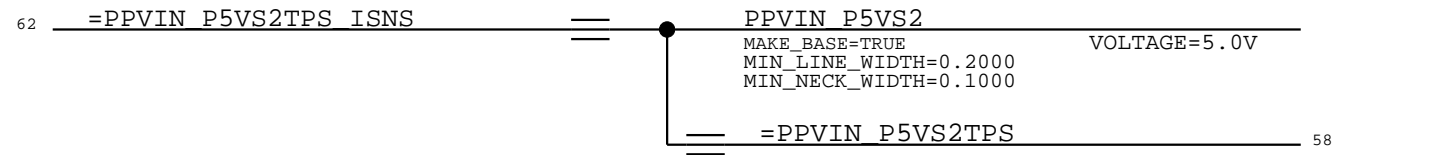
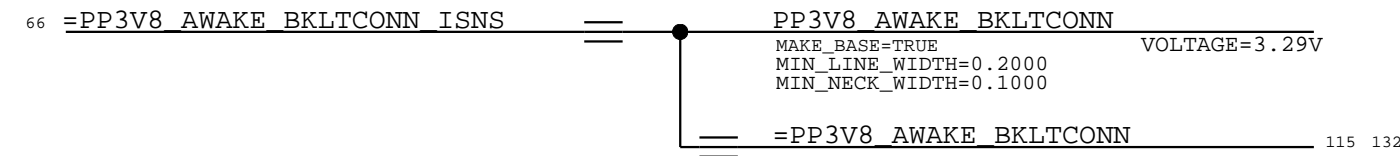
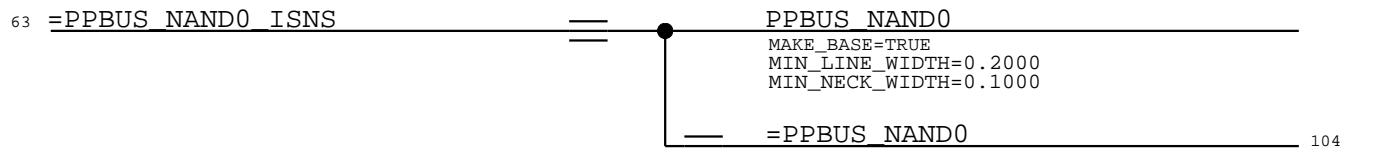
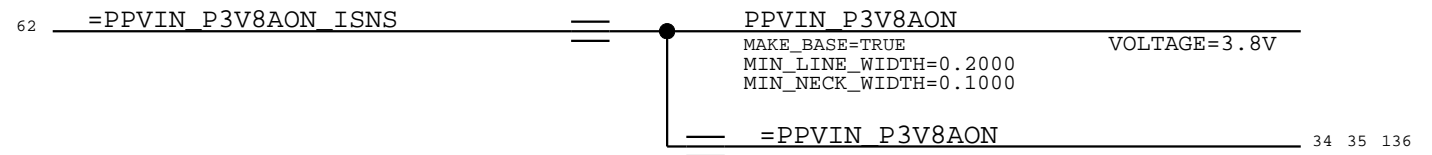
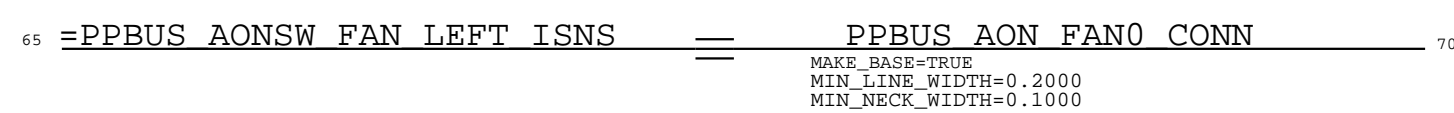
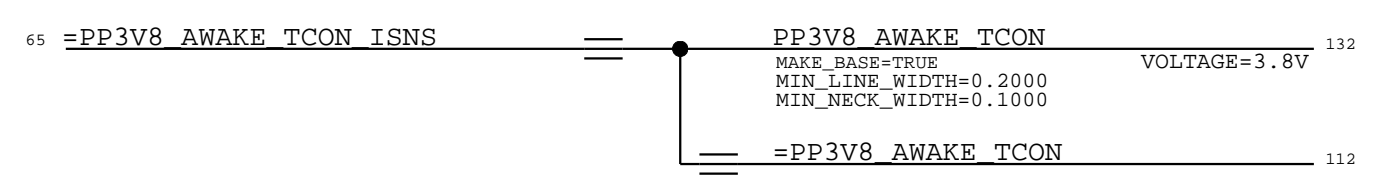
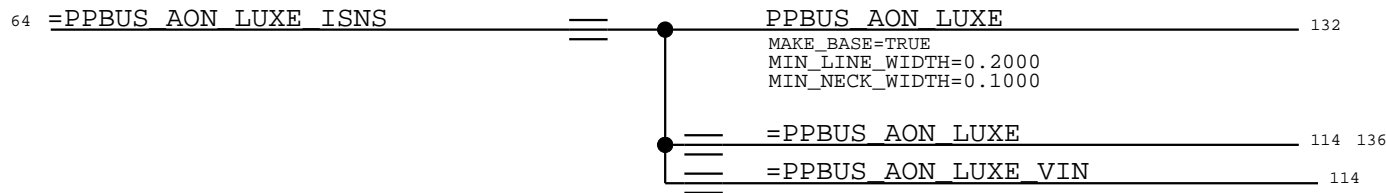
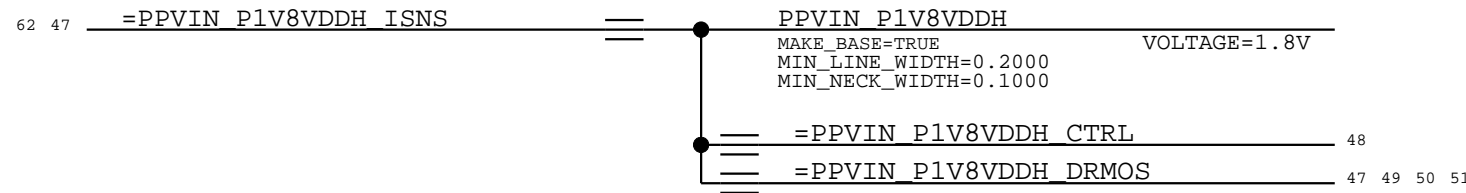
KEYBOARD BACKLIGHT




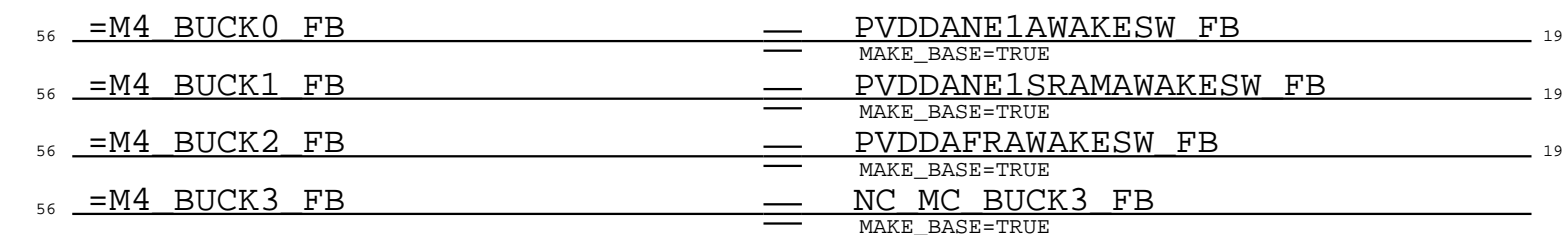
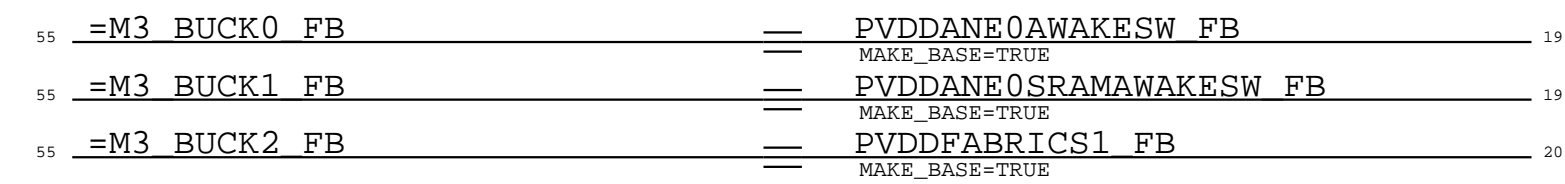
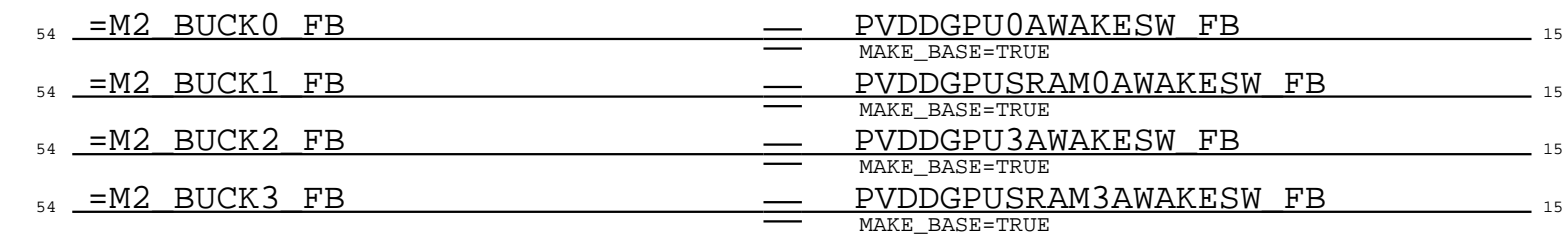
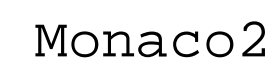
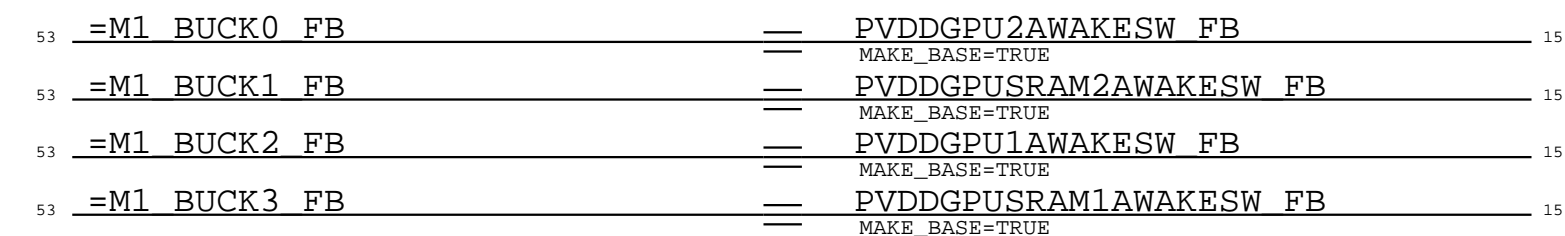
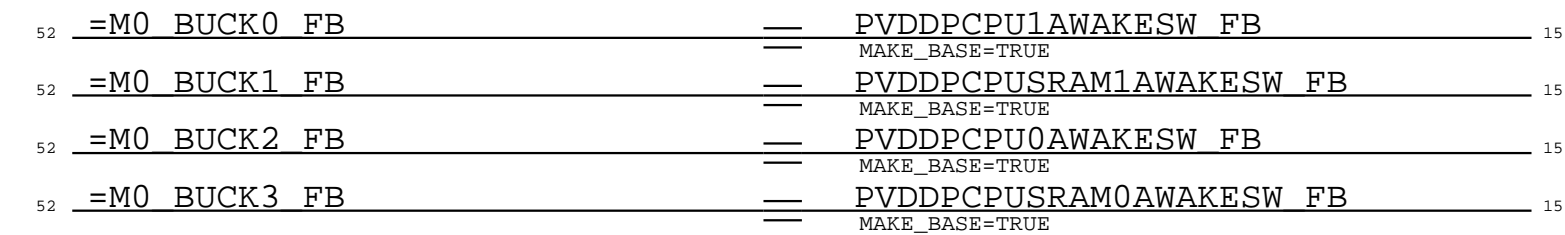
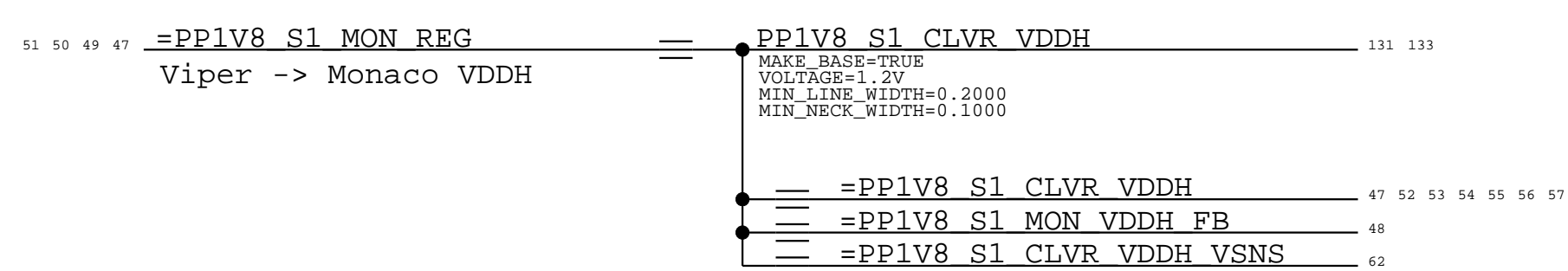
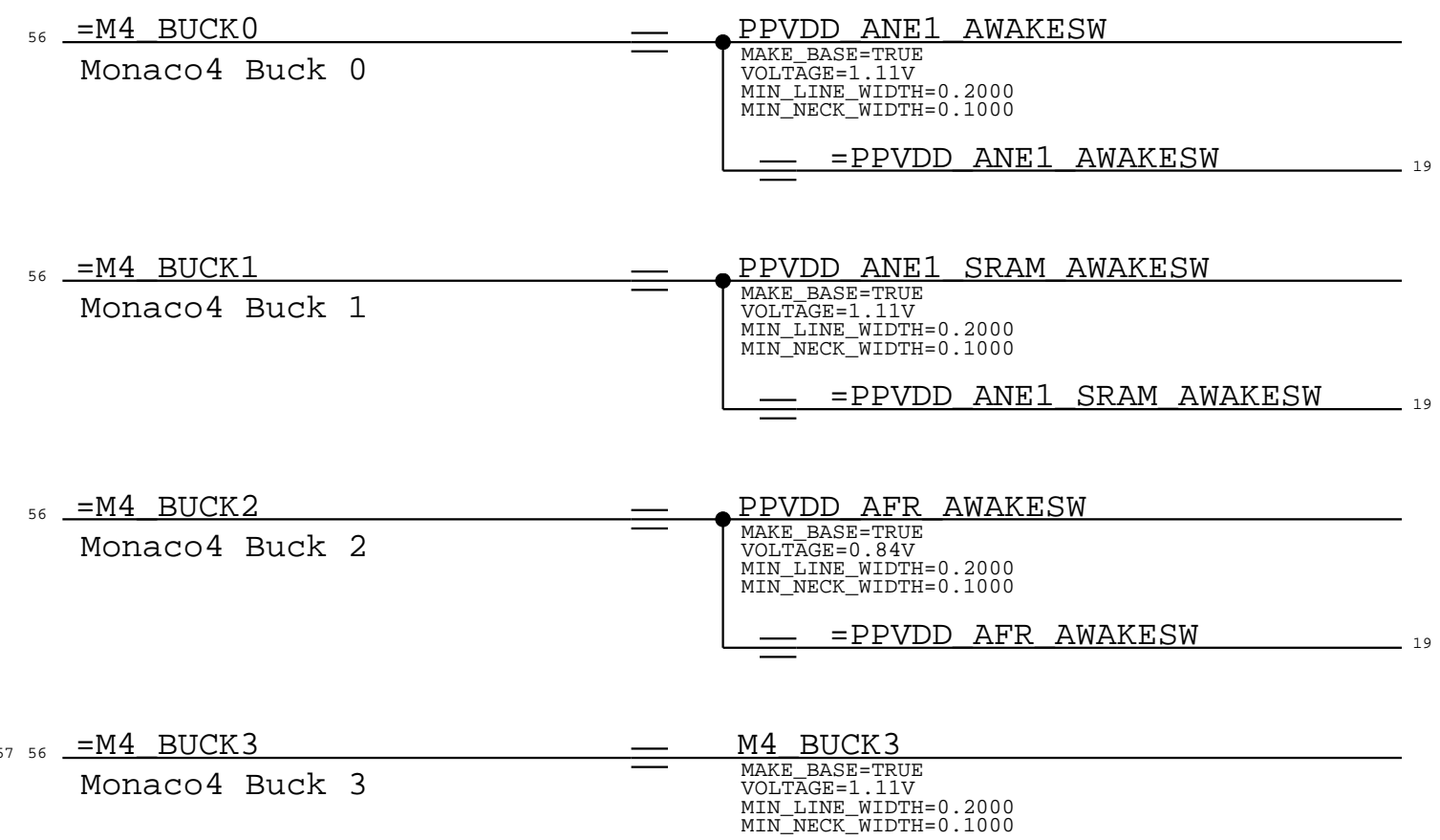
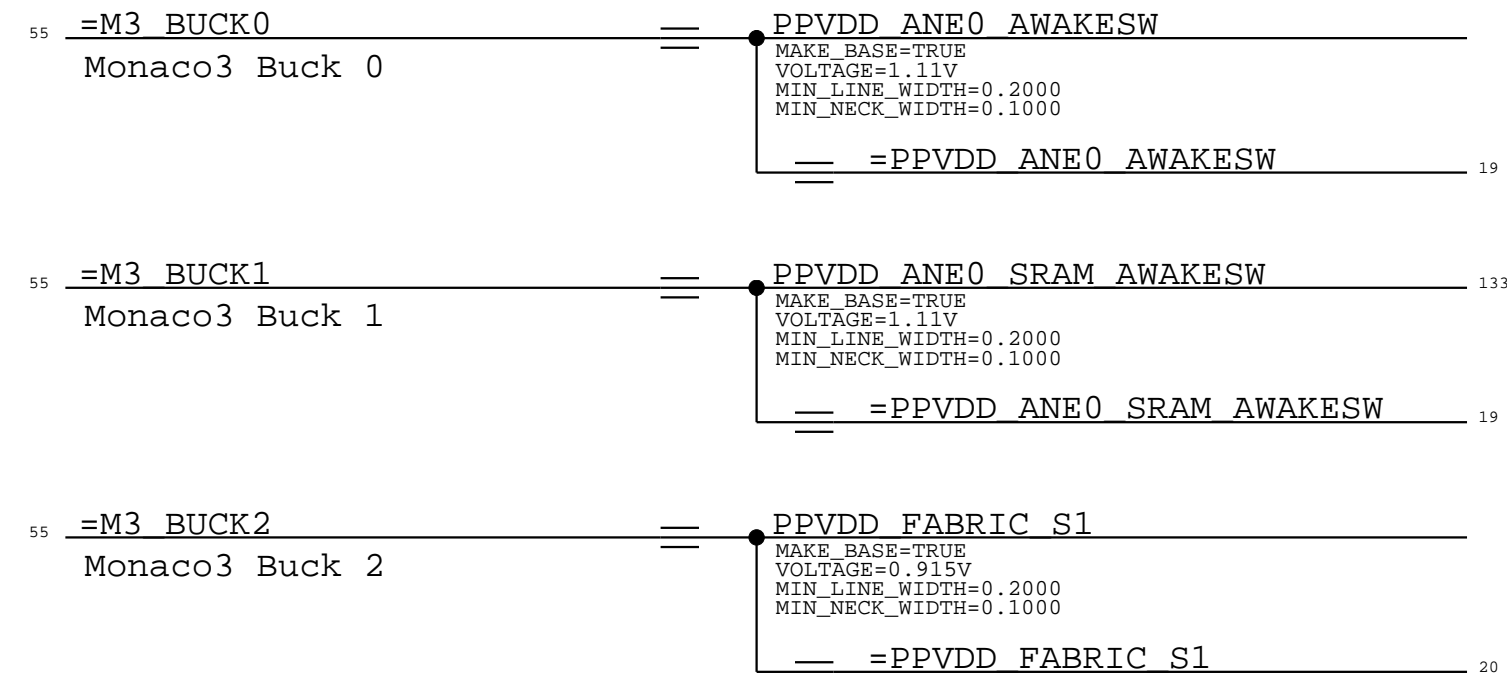
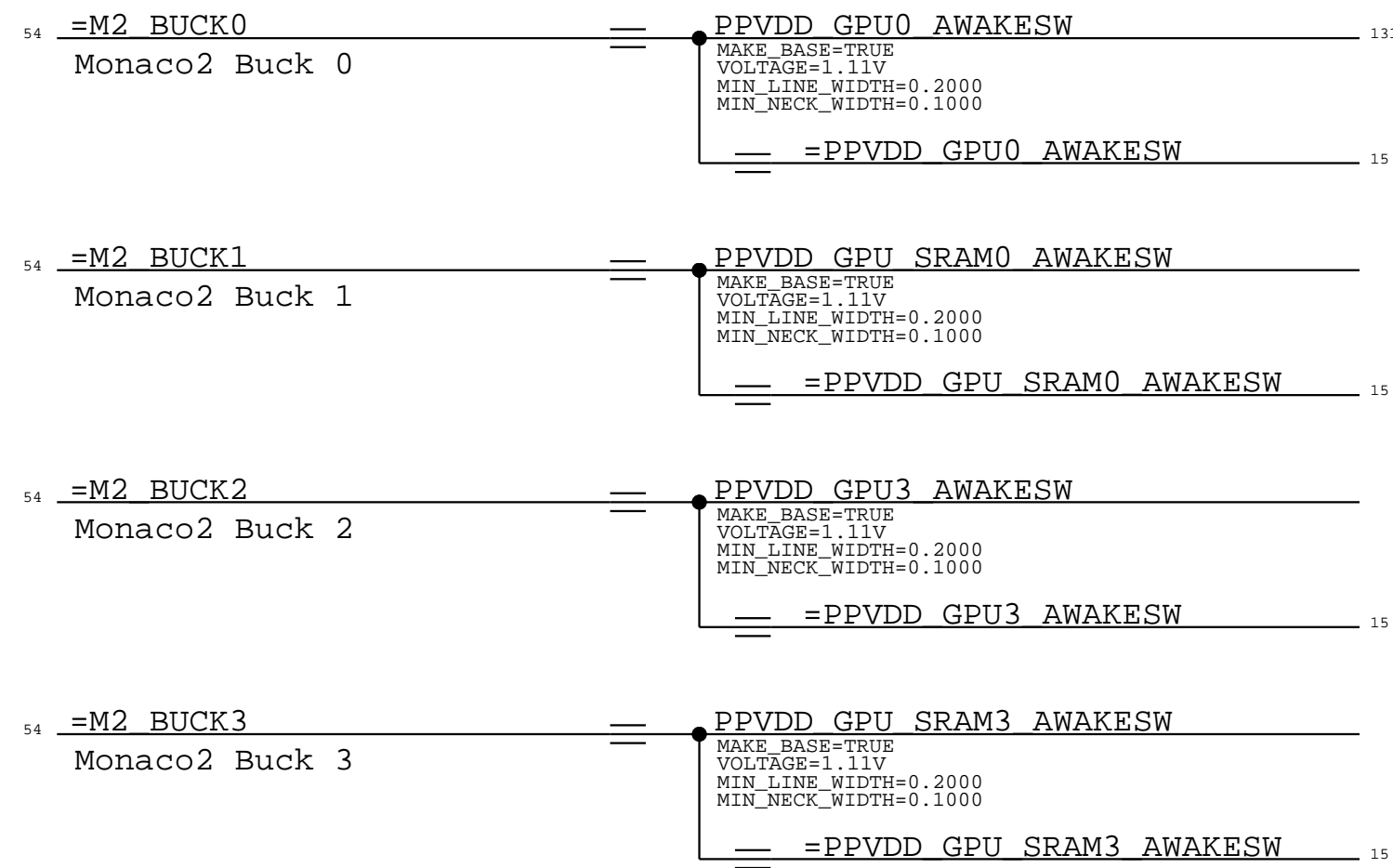
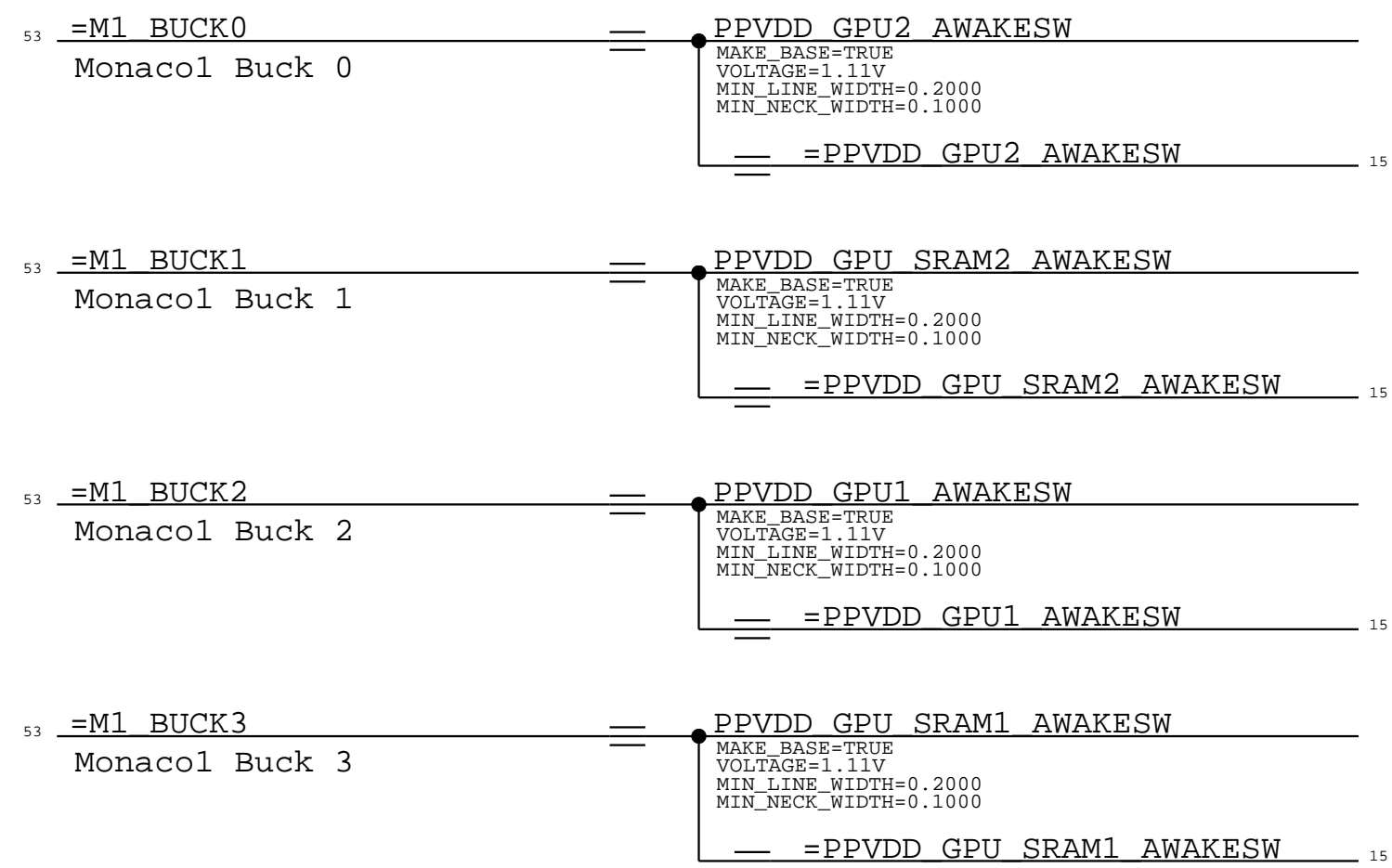
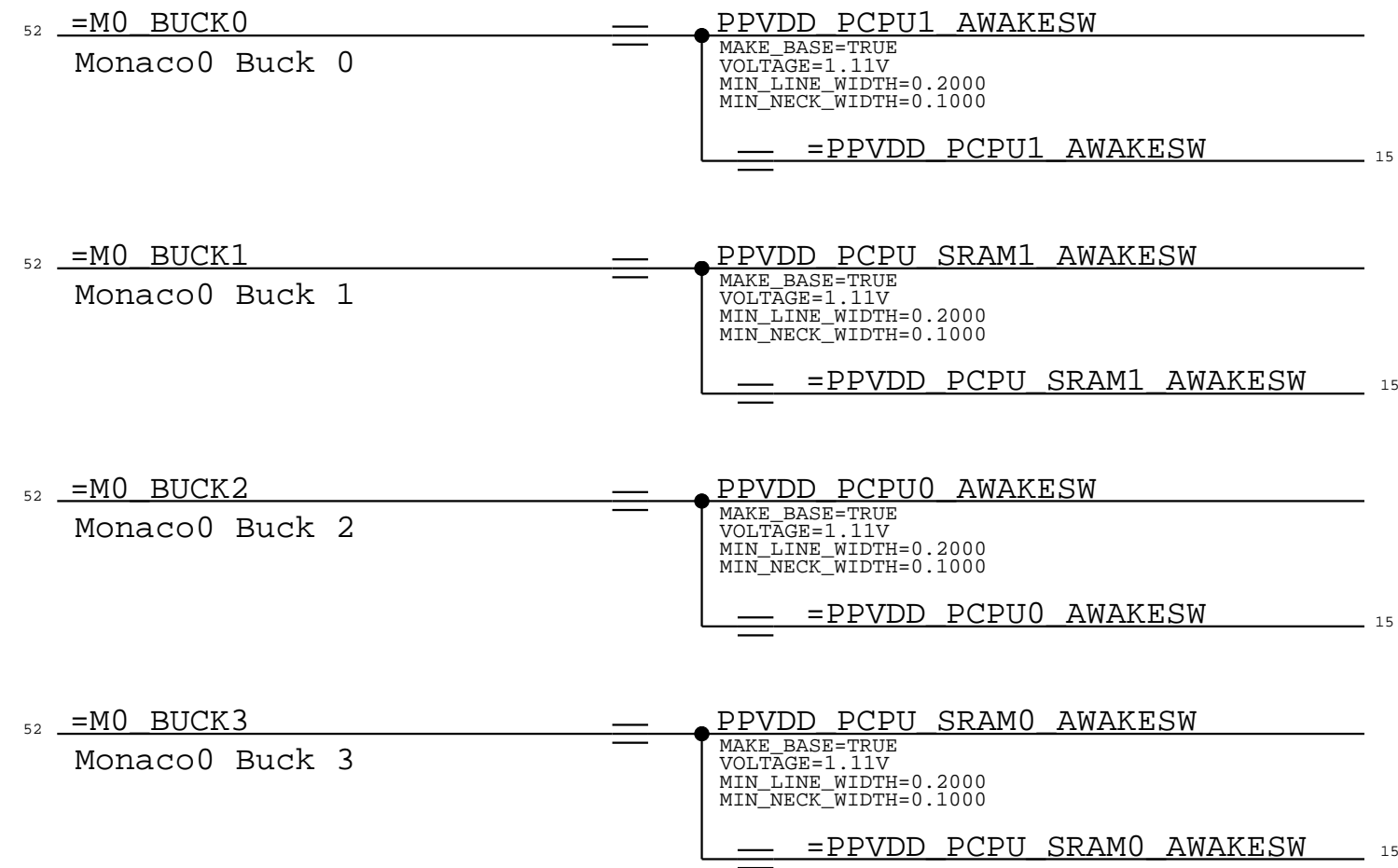
PBUS FAN SWITCH ALIAS

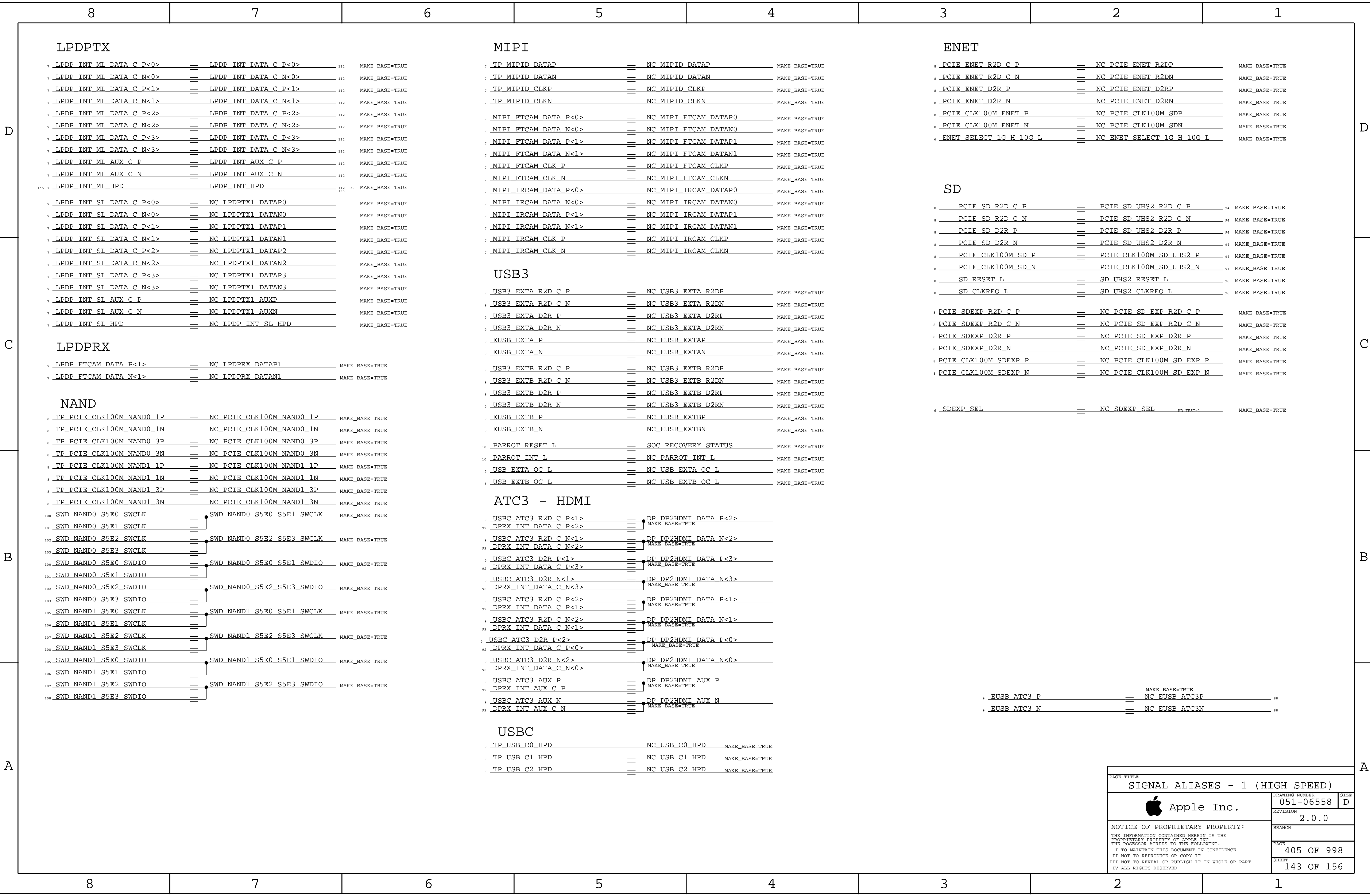


OUTPUT SENSOR ALIASES



PAGE TITLE			
POWER ALIASES 2			
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		PAGE	401 OF 998
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Internal signal aliases - Must be configured on project pages per notes below.

Internal signal aliases - Copied or debug circuitry added between.


SOC, series caps				BBR A side				BBR B side				Connector			
71	IN	USBC ATC0 R2D P<1>	MAKP_BASE=TRUE	==	=USBC ATC0 R2D P<1>	OUT	71	71	IN	=USBC0 R2D CR P<1>	MAKP_BASE=TRUE	==	USBC0 R2D CR P<1>	OUT	77
71	IN	USBC ATC0 R2D N<1>	MAKP_BASE=TRUE	==	=USBC ATC0 R2D N<1>	OUT	71	71	IN	=USBC0 R2D CR N<1>	MAKP_BASE=TRUE	==	USBC0 R2D CR N<1>	OUT	77
71	IN	USBC ATC0 R2D P<2>	MAKP_BASE=TRUE	==	=USBC ATC0 R2D P<2>	OUT	71	71	IN	=USBC0 R2D CR P<2>	MAKP_BASE=TRUE	==	USBC0 R2D CR P<2>	OUT	77
71	IN	USBC ATC0 R2D N<2>	MAKP_BASE=TRUE	==	=USBC ATC0 R2D N<2>	OUT	71	71	IN	=USBC0 R2D CR N<2>	MAKP_BASE=TRUE	==	USBC0 R2D CR N<2>	OUT	77
71	IN	USBC ATC0 D2R C P<1>	MAKP_BASE=TRUE	==	=USBC ATC0 D2R C P<1>	BT	71	71	IN	=USBC0 D2R P<1>	MAKP_BASE=TRUE	==	USBC0 D2R P<1>	BT	77
71	IN	USBC ATC0 D2R C N<1>	MAKP_BASE=TRUE	==	=USBC ATC0 D2R C N<1>	BT	71	71	IN	=USBC0 D2R N<1>	MAKP_BASE=TRUE	==	USBC0 D2R N<1>	BT	77
71	IN	USBC ATC0 D2R C P<2>	MAKP_BASE=TRUE	==	=USBC ATC0 D2R C P<2>	BT	71	71	IN	=USBC0 D2R P<2>	MAKP_BASE=TRUE	==	USBC0 D2R P<2>	BT	77
71	IN	USBC ATC0 D2R C N<2>	MAKP_BASE=TRUE	==	=USBC ATC0 D2R C N<2>	BT	71	71	IN	=USBC0 D2R N<2>	MAKP_BASE=TRUE	==	USBC0 D2R N<2>	BT	77
72	IN	USBC ATC1 R2D P<1>	MAKP_BASE=TRUE	==	=USBC ATC1 R2D P<1>	OUT	72	72	IN	=USBC1 R2D CR P<1>	MAKP_BASE=TRUE	==	USBC1 R2D CR P<1>	OUT	77
72	IN	USBC ATC1 R2D N<1>	MAKP_BASE=TRUE	==	=USBC ATC1 R2D N<1>	OUT	72	72	IN	=USBC1 R2D CR N<1>	MAKP_BASE=TRUE	==	USBC1 R2D CR N<1>	OUT	77
72	IN	USBC ATC1 R2D P<2>	MAKP_BASE=TRUE	==	=USBC ATC1 R2D P<2>	OUT	72	72	IN	=USBC1 R2D CR P<2>	MAKP_BASE=TRUE	==	USBC1 R2D CR P<2>	OUT	77
72	IN	USBC ATC1 R2D N<2>	MAKP_BASE=TRUE	==	=USBC ATC1 R2D N<2>	OUT	72	72	IN	=USBC1 R2D CR N<2>	MAKP_BASE=TRUE	==	USBC1 R2D CR N<2>	OUT	77
72	IN	USBC ATC1 D2R C P<1>	MAKP_BASE=TRUE	==	=USBC ATC1 D2R C P<1>	BT	72	72	IN	=USBC1 D2R P<1>	MAKP_BASE=TRUE	==	USBC1 D2R P<1>	BT	77
72	IN	USBC ATC1 D2R C N<1>	MAKP_BASE=TRUE	==	=USBC ATC1 D2R C N<1>	BT	72	72	IN	=USBC1 D2R N<1>	MAKP_BASE=TRUE	==	USBC1 D2R N<1>	BT	77
72	IN	USBC ATC1 D2R C P<2>	MAKP_BASE=TRUE	==	=USBC ATC1 D2R C P<2>	BT	72	72	IN	=USBC1 D2R P<2>	MAKP_BASE=TRUE	==	USBC1 D2R P<2>	BT	77
72	IN	USBC ATC1 D2R C N<2>	MAKP_BASE=TRUE	==	=USBC ATC1 D2R C N<2>	BT	72	72	IN	=USBC1 D2R N<2>	MAKP_BASE=TRUE	==	USBC1 D2R N<2>	BT	77
80	IN	USBC ATC2 R2D LS P<1>	MAKP_BASE=TRUE	==	=USBC ATC2 R2D LS P<1>	OUT	80	80	IN	=USBC2 R2D CR P<1>	MAKP_BASE=TRUE	==	USBC2 R2D CR P<1>	OUT	84
80	IN	USBC ATC2 R2D LS N<1>	MAKP_BASE=TRUE	==	=USBC ATC2 R2D LS N<1>	OUT	80	80	IN	=USBC2 R2D CR N<1>	MAKP_BASE=TRUE	==	USBC2 R2D CR N<1>	OUT	84
80	IN	USBC ATC2 R2D LS P<2>	MAKP_BASE=TRUE	==	=USBC ATC2 R2D LS P<2>	OUT	80	80	IN	=USBC2 R2D CR P<2>	MAKP_BASE=TRUE	==	USBC2 R2D CR P<2>	OUT	84
80	IN	USBC ATC2 R2D LS N<2>	MAKP_BASE=TRUE	==	=USBC ATC2 R2D LS N<2>	OUT	80	80	IN	=USBC2 R2D CR N<2>	MAKP_BASE=TRUE	==	USBC2 R2D CR N<2>	OUT	84
80	IN	USBC ATC2 D2R LS C P<1>	MAKP_BASE=TRUE	==	=USBC ATC2 D2R LS C P<1>	BT	80	80	IN	=USBC2 D2R P<1>	MAKP_BASE=TRUE	==	USBC2 D2R P<1>	BT	84
80	IN	USBC ATC2 D2R LS C N<1>	MAKP_BASE=TRUE	==	=USBC ATC2 D2R LS C N<1>	BT	80	80	IN	=USBC2 D2R N<1>	MAKP_BASE=TRUE	==	USBC2 D2R N<1>	BT	84
80	IN	USBC ATC2 D2R LS C P<2>	MAKP_BASE=TRUE	==	=USBC ATC2 D2R LS C P<2>	BT	80	80	IN	=USBC2 D2R P<2>	MAKP_BASE=TRUE	==	USBC2 D2R P<2>	BT	84
80	IN	USBC ATC2 D2R LS C N<2>	MAKP_BASE=TRUE	==	=USBC ATC2 D2R LS C N<2>	BT	80	80	IN	=USBC2 D2R N<2>	MAKP_BASE=TRUE	==	USBC2 D2R N<2>	BT	84

Caps and connector must be aliased to BBR signals.
BBR lanes 1 and 2 can be swapped, both pairs, both sides - all or nothing.
BBR inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USB2 ATC1 LS P	MAKP_BASE=TRUE	==	=USB2 ATC1 LS P	78 88
USB2 ATC1 LS N	MAKP_BASE=TRUE	==	=USB2 ATC1 LS N	78 88
USB2 ATC2 LS P	MAKP_BASE=TRUE	==	=USB2 ATC2 LS P	85 88
USB2 ATC2 LS N	MAKP_BASE=TRUE	==	=USB2 ATC2 LS N	85 88


EUSB ATC0 P	MAKP_BASE=TRUE	==	=EUSB ATC0 P	BT 78
EUSB ATC0 N	MAKP_BASE=TRUE	==	=EUSB ATC0 N	BT 78
EUSB ATC1 P	MAKP_BASE=TRUE	==	=EUSB ATC1 P	BT 78
EUSB ATC1 N	MAKP_BASE=TRUE	==	=EUSB ATC1 N	BT 78
EUSB ATC2 P	MAKP_BASE=TRUE	==	=EUSB ATC2 P	BT 85
EUSB ATC2 N	MAKP_BASE=TRUE	==	=EUSB ATC2 N	BT 85

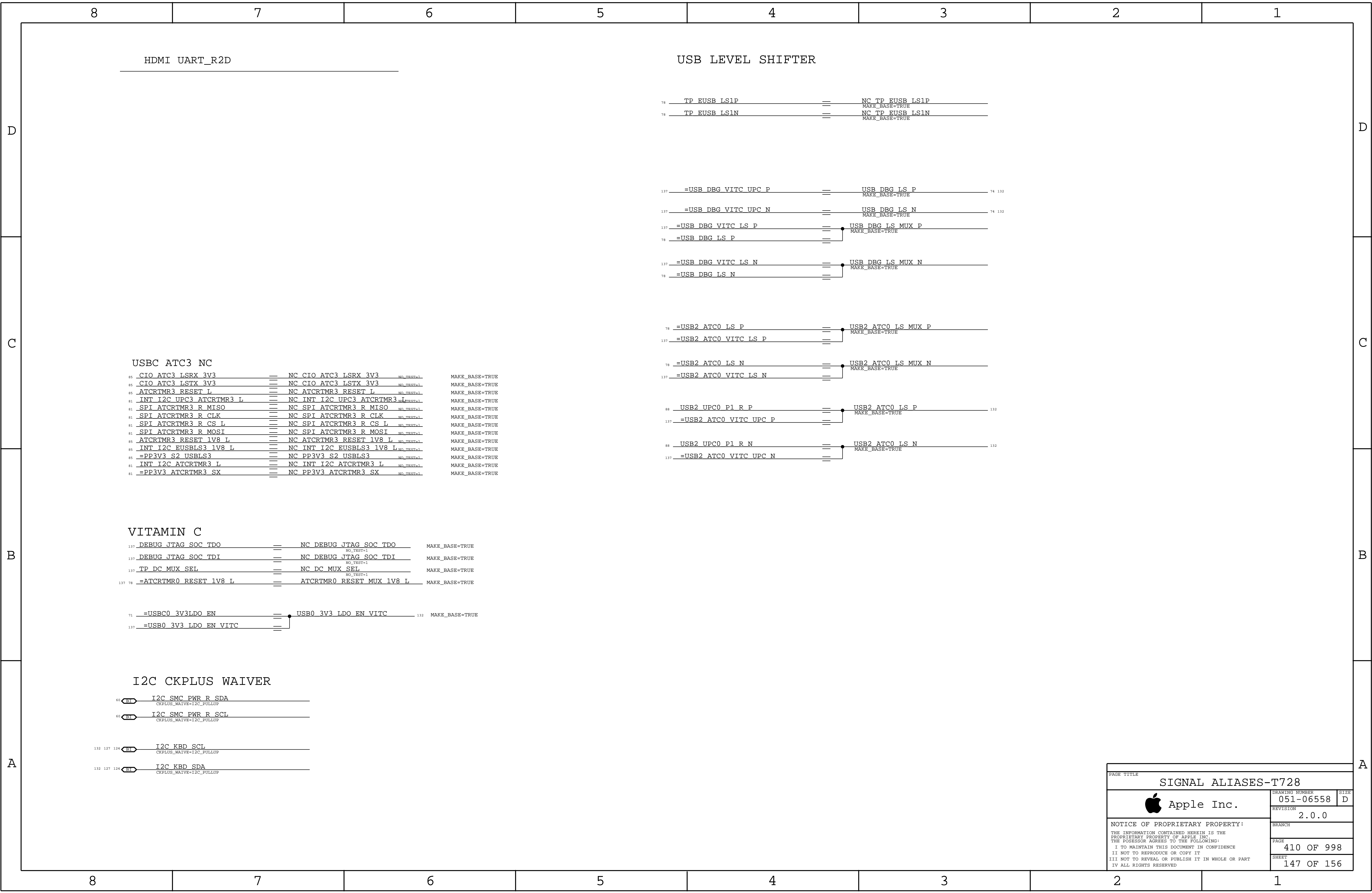
133 76	IN	USBC1 3V3LDO EN	MAKP_BASE=TRUE	==	=USBC1 3V3LDO EN	OUT 72
133 83	IN	USBC2 3V3LDO EN	MAKP_BASE=TRUE	==	=USBC2 3V3LDO EN	OUT 80

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	6	OUT I2C ENET_SDA	==	NC I2C ENET_SDA MAKE_BASE=TRUE					
	AP_I2C6								
	6	IN I2C USBA LS_SCL	==	NC I2C USBA LS_SCL MAKE_BASE=TRUE					
	6	OUT I2C USBA LS_SDA	==	NC I2C USBA LS_SDA MAKE_BASE=TRUE					
A	118	IN TDM CODEC MCLK	==	NC TDM CODEC MCLK MAKE_BASE=TRUE NO_TEST=1					
	85	IN I2C UPC3 ATCRTMR3_SDA	==	NC I2C UPC3 ATCRTMR3_SDA MAKE_BASE=TRUE NO_TEST=1					
	85	OUT I2C UPC3 ATCRTMR3_SCL	==	NC I2C UPC3 ATCRTMR3_SCL MAKE_BASE=TRUE NO_TEST=1					


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D	ISP GPIO		D2D IO			NC SPN's		
	<div><div><div>7</div><div>IRCAM RESET L</div><div></div><div>MAKE_BASE=TRUE</div><div>NC IRCAM RESET L</div><div></div></div><div><div>7</div><div>CAM PMU RESET L</div><div></div><div>NC CAM PMU RESET L</div><div></div></div></div>		<div><div><div>5</div><div>TP A2A SYNC ACK</div><div></div><div>NC A2A SYNC ACK</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP A2A SYNC REQ</div><div></div><div>NC A2A SYNC REQ</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP A2A WAKEUP</div><div></div><div>NC A2A WAKEUP</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP C2C CLK 24 IN</div><div></div><div>NC C2C CLK 24 IN</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP C2C CLK 24 OUT</div><div></div><div>NC C2C CLK 24 OUT</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP C2C TIME SYNC IN</div><div></div><div>NC C2C TIME SYNC IN</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP C2C TIME SYNC OUT</div><div></div><div>NC C2C TIME SYNC OUT</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG TX REQ</div><div></div><div>NC GTRIG TX REQ</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG TX ACK</div><div></div><div>NC GTRIG TX ACK</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG TX LNO</div><div></div><div>NC GTRIG TX LNO</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG TX LNI</div><div></div><div>NC GTRIG TX LNI</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG RX REQ</div><div></div><div>NC GTRIG RX REQ</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG RX ACK</div><div></div><div>NC GTRIG RX ACK</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG RX LNO</div><div></div><div>NC GTRIG RX LNO</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP GTRIG RX LNI</div><div></div><div>NC GTRIG RX LNI</div><div>MAKE_BASE=TRUE</div></div></div>			<div><div><div>7</div><div>TP DISP TOUCH BSYNC0</div><div></div><div>MAKE_BASE=TRUE</div><div>NC DISP TOUCH BSYNC0</div><div></div></div><div><div>7</div><div>TP DISP TOUCH BSYNC1</div><div></div><div>NC DISP TOUCH BSYNC1</div><div></div></div><div><div>7</div><div>TP DISP TOUCH EB</div><div></div><div>NC DISP TOUCH EB</div><div></div></div><div><div>7</div><div>TP DFR DISP TE</div><div></div><div>NC DFR DISP TE</div><div></div></div></div>		
	AOP IO							
	<div><div><div>10</div><div>IRCAM PROX INT L</div><div></div><div>NC IRCAM PROX INT L</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP GPIO1</div><div></div><div>NC AOP GPIO1</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP GPIO5</div><div></div><div>NC AOP GPIO5</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP I2CM1_SCL</div><div></div><div>NC AOP I2CM1_SCL</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP I2CM1_SDA</div><div></div><div>NC AOP I2CM1_SDA</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP PDM DMIC CLK1</div><div></div><div>NC PDM DMIC CLK1</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP I2S0 MCK</div><div></div><div>NC AOP I2S0 MCK</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP I2S0 LRCK</div><div></div><div>NC AOP I2S0 LRCK</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP I2S0 DOUT</div><div></div><div>NC AOP I2S0 DOUT</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP I2S0 DIN</div><div></div><div>NC AOP I2S0 DIN</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP I2S0 BCLK</div><div></div><div>NC AOP I2S0 BCLK</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP PDM DMIC DATA1</div><div></div><div>NC PDM DMIC DATA1</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP UART2 R2D</div><div></div><div>NC AOP UART2 R2D</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP UART2 D2R</div><div></div><div>NC AOP UART2 D2R</div><div>MAKE_BASE=TRUE</div></div><div><div>10</div><div>TP AOP GPIO0</div><div></div><div>SOC DOMAIN AGPIO AOP0</div><div>MAKE_BASE=TRUE 146</div></div></div>					<div><div><div>7</div><div>CAM PMU CLK24M R</div><div></div><div>MAKE_BASE=TRUE</div><div>NC CAM PMU CLK24M R</div><div></div></div><div><div>7</div><div>TP SENSOR1 CLK</div><div></div><div>NC SENSOR1 CLK</div><div></div></div><div><div>7</div><div>TP SENSOR2 CLK</div><div></div><div>NC SENSOR2 CLK</div><div></div></div><div><div>7</div><div>TP SENSOR3 CLK</div><div></div><div>NC SENSOR3 CLK</div><div></div></div></div>		
	CLVR GPIO		NAND					
	<div><div><div>5</div><div>TP CLVR GPIO1</div><div></div><div>NC CLVR GPIO1</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP CLVR GPIO2</div><div></div><div>NC CLVR GPIO2</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP CLVR GPIO3</div><div></div><div>NC CLVR GPIO3</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP CLVR GPIO4</div><div></div><div>NC CLVR GPIO4</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP CLVR GPIO5</div><div></div><div>NC CLVR GPIO5</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP CLVR GPIO6</div><div></div><div>NC CLVR GPIO6</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP CLVR GPIO7</div><div></div><div>SOC DOMAIN GPIO GRP1 0</div><div>MAKE_BASE=TRUE 146</div></div><div><div>5</div><div>TP CLVR GPIO8</div><div></div><div>NC CLVR GPIO8</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP CLVR GPIO9</div><div></div><div>NC CLVR GPIO9</div><div>MAKE_BASE=TRUE</div></div></div>		<div><div><div>8</div><div>TP SSD RESET0 L</div><div></div><div>SOC DOMAIN HGPIO GRP0 0</div><div>MAKE_BASE=TRUE</div></div><div><div>8</div><div>TP SSD RESET1 7 L</div><div></div><div>SOC DOMAIN HGPIO GRP0 1</div><div>MAKE_BASE=TRUE</div></div></div>					
C			ISP SPMI					
			<div><div><div>7</div><div>SPMI ISP CAM CLK R</div><div></div><div>NC SPMI ISP CAM CLK R</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>SPMI ISP CAM DATA R</div><div></div><div>NC SPMI ISP CAM DATA R</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP ISP I2C0_SCL</div><div></div><div>NC ISP I2C0_SCL</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP ISP I2C0_SDA</div><div></div><div>NC ISP I2C0_SDA</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP ISP I2C1_SCL</div><div></div><div>NC ISP I2C1_SCL</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP ISP I2C1_SDA</div><div></div><div>NC ISP I2C1_SDA</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP ISP I2C3_SCL</div><div></div><div>NC ISP I2C3_SCL</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP ISP I2C3_SDA</div><div></div><div>NC ISP I2C3_SDA</div><div>MAKE_BASE=TRUE</div></div></div>					
			<div><div><div>7</div><div>TP ISP GPIO3</div><div></div><div>SOC DOMAIN GPIO GRP1 2</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP SPMI1 ISP CLK</div><div></div><div>NC SPMI1 ISP CLK</div><div>MAKE_BASE=TRUE</div></div><div><div>7</div><div>TP SPMI1 ISP DATA</div><div></div><div>NC SPMI1 ISP DATA</div><div>MAKE_BASE=TRUE</div></div></div>					
	SMC GPIO		VIPER PWM					
	<div><div><div>10</div><div>ACDC BURST EN L</div><div></div><div>NC ACDC BURST EN L</div><div></div></div><div><div>10</div><div>ACDC ID</div><div></div><div>NC ACDC ID</div><div></div></div><div><div>10</div><div>PSU TBD3</div><div></div><div>NC PSU TBD3</div><div></div></div><div><div>10</div><div>TP SMC GPIO1</div><div></div><div>SOC DOMAIN MGPIO AOP1</div><div>146</div></div><div><div>10</div><div>TP SMC GPIO2</div><div></div><div>NC SMC GPIO2</div><div></div></div><div><div>10</div><div>TP SMC GPIO3</div><div></div><div>NC SMC GPIO3</div><div></div></div><div><div>10</div><div>TP SMC GPIO4</div><div></div><div>NC SMC GPIO4</div><div></div></div><div><div>10</div><div>TP SMC I2CM6_SCL</div><div></div><div>NC SMC I2CM6_SCL</div><div></div></div><div><div>10</div><div>TP SMC I2CM6_SDA</div><div></div><div>NC SMC I2CM6_SDA</div><div></div></div></div>		<div><div><div>48</div><div>P1V8VDDH DRMos PWM6</div><div></div><div>NC P1V8VDDH DRMos PWM6</div><div>MAKE_BASE=TRUE</div></div><div><div>48</div><div>P1V8VDDH DRMos PWM7</div><div></div><div>NC P1V8VDDH DRMos PWM7</div><div>MAKE_BASE=TRUE</div></div><div><div>48</div><div>P1V8VDDH DRMos PWM8</div><div></div><div>NC P1V8VDDH DRMos PWM8</div><div>MAKE_BASE=TRUE</div></div></div>					
B	NUB GPIO		NC SPN's			SOC GPIO TP's BY DOMAIN		
	<div><div><div>10</div><div>TITUS B2B DETECT L</div><div></div><div>MAKE_BASE=TRUE</div><div>SOC DOMAIN NGPIO AOP1 2</div><div>146</div></div><div><div>10</div><div>TP NUB CLK OUT0</div><div></div><div>SOC DOMAIN NGPIO AOP1 0</div><div>146</div></div><div><div>10</div><div>TP NUB CLK OUT1</div><div></div><div>SOC DOMAIN NGPIO AOP1 1</div><div>146</div></div><div><div>10</div><div>TP NUB SWD TMS3</div><div></div><div>NC NUB SWD TMS3</div><div></div></div><div><div>10</div><div>TP NUB JTAG SLV TCK</div><div></div><div>NC NUB JTAG SLV TCK</div><div></div></div><div><div>10</div><div>TP NUB JTAG SLV TMS</div><div></div><div>NC NUB JTAG SLV TMS</div><div></div></div><div><div>10</div><div>TP NUB JTAG SLV TDI</div><div></div><div>NC NUB JTAG SLV TDI</div><div></div></div><div><div>10</div><div>TP NUB JTAG SLV TDO</div><div></div><div>NC NUB JTAG SLV TDO</div><div></div></div><div><div>10</div><div>TP NUB JTAG SLV TRSTN</div><div></div><div>NC NUB JTAG SLV TRSTN</div><div></div></div></div>		<div><div><div>5</div><div>TP PAD MTR ANALOG TESTP</div><div></div><div>NC PAD MTR ANALOG TESTP</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP PAD MTR ANALOG TESTN</div><div></div><div>NC PAD MTR ANALOG TESTN</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP PAD MTR VREFP</div><div></div><div>NC PAD MTR VREFP</div><div>MAKE_BASE=TRUE</div></div><div><div>5</div><div>TP PAD MTR VREFN</div><div></div><div>NC PAD MTR VREFN</div><div>MAKE_BASE=TRUE</div></div></div>			<div><div><div>146</div><div>SOC DOMAIN GPIO GRP0</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ01</div><div><div>146</div><div>SOC DOMAIN NGPIO AOP1 0</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ02</div><div><div>146</div><div>SOC DOMAIN GPIO GRP1 0</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ03</div><div><div>146</div><div>SOC DOMAIN NGPIO AOP1 1</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ04</div><div><div>146</div><div>SOC DOMAIN GPIO GRP1 1</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ05</div><div><div>146</div><div>SOC DOMAIN NGPIO AOP1 2</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ06</div><div><div>146</div><div>SOC DOMAIN GPIO GRP1 2</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ07</div><div><div>146</div><div>SOC DOMAIN HGPIO GRP0 0</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ08</div><div><div>146</div><div>SOC DOMAIN AGPIO AOP0</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ09</div><div><div>146</div><div>SOC DOMAIN HGPIO GRP0 1</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ10</div><div><div>146</div><div>SOC DOMAIN MGPIO AOP1</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ11</div><div><div>146</div><div>SOC DOMAIN SGPIO GRP1</div><div><div>P2MM</div><div>1</div><div>SH</div><div>TP</div></div><div>PLACE_SIDE=TOP</div></div><div>PPZZ12</div></div>		
A	ENET GPIO					A		
	<div><div><div>6</div><div>ENET SYNC 1588</div><div></div><div>MAKE_BASE=TRUE</div><div>NC ENET SYNC 1588</div><div></div></div></div>					<div><div><div>806</div><div>TP AP GPIO28</div><div></div><div>NC AP GPIO28</div><div>MAKE_BASE=TRUE</div></div><div><div>806</div><div>TP AP GPIO29</div><div></div><div>NC AP GPIO29</div><div>MAKE_BASE=TRUE</div></div><div><div>806</div><div>TP AP GPIO30</div><div></div><div>NC AP GPIO30</div><div>MAKE_BASE=TRUE</div></div><div><div>806</div><div>TP AP GPIO31</div><div></div><div>NC AP GPIO31</div><div>MAKE_BASE=TRUE</div></div><div><div>806</div><div>TP AP GPIO32</div><div></div><div>NC AP GPIO32</div><div>MAKE_BASE=TRUE</div></div><div><div>806</div><div>TP SOC MASTER SYNC GEN 2</div><div></div><div>SOC DOMAIN GPIO GRP0</div><div>146</div><div>MAKE_BASE=TRUE</div></div><div><div>806</div><div>TP AP GPIO34</div><div></div><div>SOC DOMAIN GPIO GRP1 1</div><div>146</div><div>MAKE_BASE=TRUE</div></div></div>		
	8	7	6	5	4	3	2	1

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SCSET RULES


DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_N1X <small>Calculate dielectric N1 spacing from starting. Minimum distance is 1 and value 2 is defined</small>	VALUES: 1, 2, 5, 10, 20, 100 2-10
A_DIELECTRIC_N1XD XY, AVL, X <small>Calculate dielectric N1 spacing for layer N1 and starting distance N1XD from N1 to N1XD</small>	VALUES: 2, 10, 100, 20, 100, 100 PLEASE USE HYBRID TABLE
A_DIELECTRIC_N1XIN N1XOUT <small>Calculate dielectric N1 spacing from starting. Minimum distance is 1 and value 2 is defined</small>	VALUES: 2, 5, 10, 20

8		7		6		5		4		3		2		1	
SOC/CPU															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
998-23492		1	SOC,CGA A0+32G,1Y,8C,LP,DEV,AX,H,S,B4183			U0600		CRITICAL	SOC:A0_32G						
998-23494		1	SOC,CGA A0+64G,1Y,8C,LP,DEV,AX,H,S,B4183			U0600		CRITICAL	SOC:A0_64G						
939-10299		1	PCBF,NANJING,X2737			U0600		CRITICAL	SOC:SOCKET						
SPACE LEFT FOR ADDITIONAL SOC APNs															
BBR IC															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
998-13316		3	IC,BURNSIDE BRIDGE,USB/TB RTIMER,BGA105			UF000,UF100,UG000		CRITICAL	ATCRTMR:DEV						
338S00561		3	IC,TBT,BBR,SLMN7,PRQ,A1,BGA105			UF000,UF100,UG000		CRITICAL	BBR:A1_PRQ						
ACE/UPC															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
353S02158		3	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123			UF400,UF500,UG400		CRITICAL	ACE2:B2						
BBR ROMs															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
341S01596		1	ROM,GARLIC-P,TBT,POC-2			UF260		CRITICAL	BBR_L_ROM:POC-2			<-LEFT			
341S01596		1	ROM,GARLIC-P,TBT,POC-2			UG260		CRITICAL	BBR_R_ROM:POC-2			<-RIGHT			
341S01830		1	ROM,ACE-P5 (VXXX) PROTO-2,X2728			U5660		CRITICAL	ACE5_ROM:T818			<-MAGSAFE			
BBR BOM ALT parts															
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:										
335S00232		335S00133		ALL											
HDMI CONNECTOR															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
514S00354		1	CONN,RCPT,HDMI,X2094			JH500		CRITICAL							
SD CARD CONNECTOR															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
514-00180		1	CONN,RCPT,SD,X2094			JK600		CRITICAL							
EUSB LEVEL SHIFTER															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
998-23161		3	IC,MACAW,CYUSB2402A0,A0,VER 2,CSF24			UF700,UF750,UG700		CRITICAL	EUSB_LS:MACAW						
OCARINA0															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
338S00600		1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56			UN400		CRITICAL	OCARINA0:A0_OTPBC						
OCARINA1															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
338S00600		1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56			UN900		CRITICAL	OCARINA1:A0_OTPBC						
SECURE ELEMENT															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
338S00630		1	IC,SN210V,B1,CERES,PROD,VER=MU,WLCSP81			U5000		CRITICAL	SE:PROD_SW_MU						
998-21255		1	IC,SN210V,B1,CERES,SW-H3,WLCSP81			U5000		CRITICAL	SE:DEV_SW_H3						
HDMI MADEA															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL	BOM OPTION						
338S00347		1	IC,HDMI,PUMA81,MCDP2920,A4,BGA117			UH700		CRITICAL							
Maverics															

PART#		QTY	DESCRIPTION		REFERENCE DESIGNATOR(S)		CRITICAL	BOM OPTION	
335S00480		1	NAND,3DV4,160GBT,XXX,8SE,256G,K,SLGA110		UN000		CRITICAL	NAND:TS-512	
335S00462		3	NAND,3DV4,128GBT,XXX,8SE,256G,T,SLGA110		UN100,UN200,UN300		CRITICAL	NAND:TS-512	
335S00437		4	NAND,3DV5,128GB,8SE,512G,H,SLGA110		UN000,UN100,UN200,UN300		CRITICAL	NAND:HY-512	
335S00436		1	NAND,3DV5,64GB,8SE,512G,H,SLGA110		UN500		CRITICAL	NAND:HY-512	
335S00464		4	NAND,3DV4,256GBT,XXX,8SE,256G,T,SLGA110		UN000,UN100,UN200,UN300		CRITICAL	NAND:TS-1TB	
335S00472		4	NAND,3DV4,256GBT,XXX,8SE,256G,SD,SLGA110		UN000,UN100,UN200,UN300		CRITICAL	NAND:WD-1TB	
335S00438		4	NAND,3DV5,256GB,8SE,512G,H,SLGA110		UN000,UN100,UN200,UN300		CRITICAL	NAND:HY-1TB	
335S00436		1	NAND,3DV5,64GB,8SE,512G,H,SLGA110		UN500		CRITICAL	NAND:HY-1TB	
335S00466		4	NAND,3DV4,512GBT,XXX,8SE,256G,T,SLGA110		UN000,UN100,UN200,UN300		CRITICAL	NAND:TS-2TB	
335S00474		4	NAND,3DV4,512GBT,XXX,8SE,256G,SD,SLGA110		UN000,UN100,UN200,UN300		CRITICAL	NAND:WD-2TB	
335S00466		8	NAND,3DV4,512GBT,XXX,8SE,256G,T,SLGA110		UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800		CRITICAL	NAND:TS-4TB	
335S00439		8	NAND,3DV5,512GB,8SE,512G,H,SLGA110		UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800		CRITICAL	NAND:HY-4TB	
335S00468		8	NAND,3DV4,1TB,XXX,8SE,512G,T,SLGA110		UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800		CRITICAL	NAND:TS-8TB	
335S00458		8	NAND,3DV5,1024GBT,8SE,512G,H,SLGA110		UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800		CRITICAL	NAND:HY-8TB	

PART#		QTY	DESCRIPTION		REFERENCE DESIGNATOR(S)		CRITICAL	BOM OPTION	
939-08815		1	PCBF,BANDIPUR,X1711		UN000,UN600		CRITICAL	NAND:SOCKET	

ACE/UPC OTP	
----> CSA 162	
ICEMAN	
----> CSA 57	
VIPER	
----> CSA 93	
MONACO	
----> CSA 101,102,103,104,105	
HDMI ROM	
----> CSA 178	

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		REVISION	2.0.0
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NAND Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00480	1	NAND,3DV4,160GBT,XXX,85E,256G,K,SLGA110	UN000	CRITICAL	NAND:TS-512
335S00462	3	NAND,3DV4,128GBT,XXX,85E,256G,T,SLGA110	UN100,UN200,UN300	CRITICAL	NAND:TS-512
335S00437	4	NAND,3DV5,128GB,85E,512G,H,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-512
335S00436	1	NAND,3DV5,64GB,85E,512G,H,SLGA110	UN500	CRITICAL	NAND:HY-512
335S00464	4	NAND,3DV4,256GBT,XXX,85E,256G,T,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-1TB
335S00472	4	NAND,3DV4,256GBT,XXX,85E,256G,SD,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-1TB
335S00438	4	NAND,3DV5,256GB,85E,512G,H,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-1TB
335S00436	1	NAND,3DV5,64GB,85E,512G,H,SLGA110	UN500	CRITICAL	NAND:HY-1TB
335S00466	4	NAND,3DV4,512GBT,XXX,85E,256G,T,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-2TB
335S00474	4	NAND,3DV4,512GBT,XXX,85E,256G,SD,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-2TB
335S00466	8	NAND,3DV4,512GBT,XXX,85E,256G,T,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:TS-4TB
335S00439	8	NAND,3DV5,512GB,85E,512G,H,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:HY-4TB
335S00468	8	NAND,3DV4,1TB,T,XXX,85E,512G,T,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:TS-8TB
335S00458	8	NAND,3DV5,1024GBT,85E,512G,H,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:HY-8TB

NAND Socket

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
939-08815	1	PCBF,BANDIPUR,X1711	UN000,UN600	CRITICAL	NAND:SOCKET

ACE/UPC OTP

----> CSA 162

ICEMAN

----> CSA 57

VIPER


----> CSA 93




MONACO

----> CSA 101,102,103,104,105

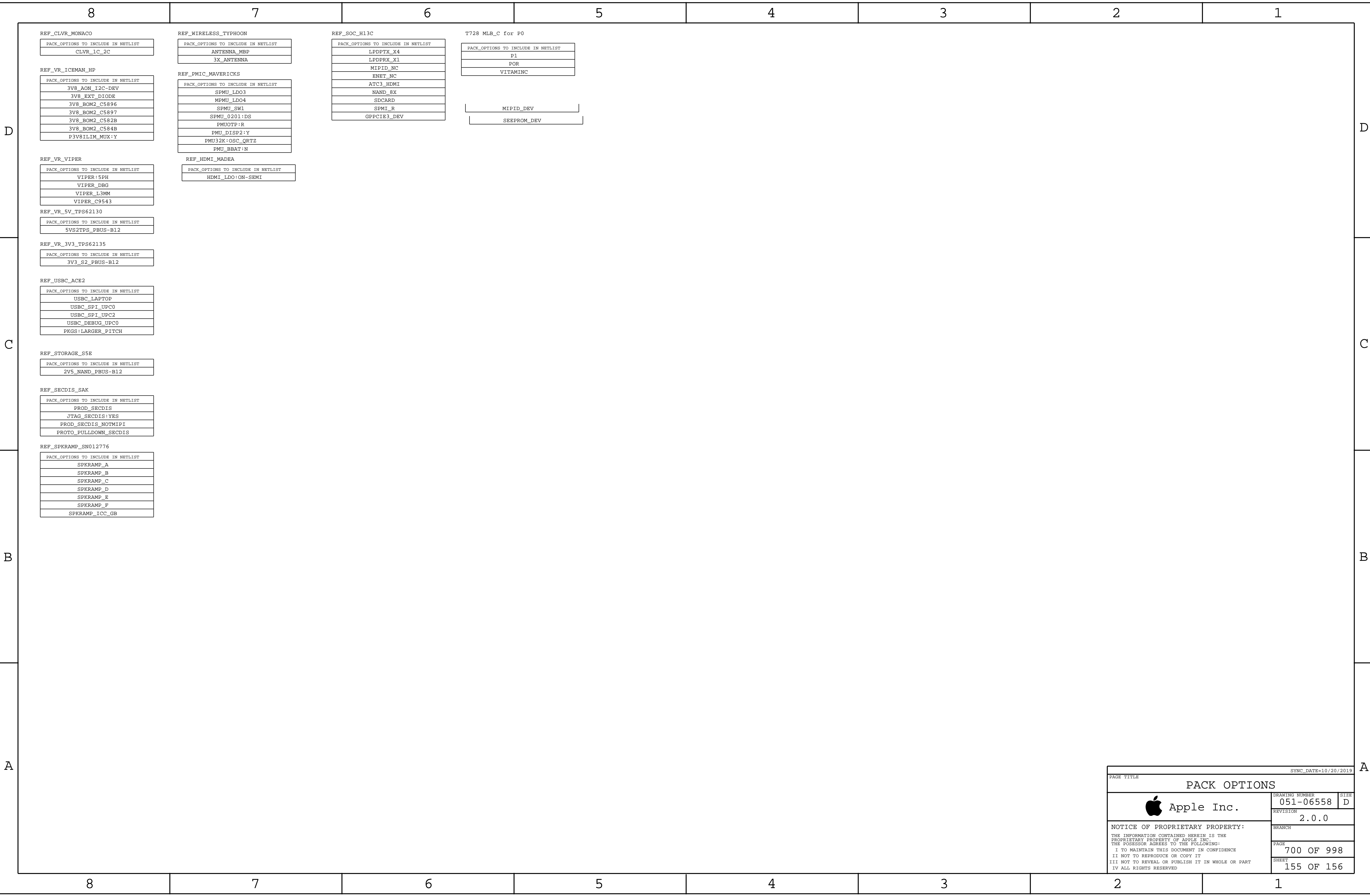
HDMI ROM

----> CSA 178

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	BOM VARIANT TABLES																																							
	BOM NUMBER	BOM NAME	BOM OPTIONS																																					
	639-14996	PCBA,MLB-C,32GB,TS-512,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-512																																					
	639-14997	PCBA,MLB-C,32GB,HY-1TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-1TB																																					
	639-14998	PCBA,MLB-C,32GB,HY-4TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-4TB																																					
	639-14999	PCBA,MLB-C,32GB,HY-512,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-512																																					
	639-15000	PCBA,MLB-C,32GB,HY-8TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-8TB																																					
	639-15001	PCBA,MLB-C,32GB,TS-1TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-1TB																																					
	639-15002	PCBA,MLB-C,32GB,TS-2TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-2TB																																					
	639-15003	PCBA,MLB-C,32GB,TS-4TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-4TB																																					
	639-15004	PCBA,MLB-C,32GB,TS-8TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-8TB																																					
	639-15005	PCBA,MLB-C,32GB,WD-1TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:WD-1TB																																					
	639-15006	PCBA,MLB-C,32GB,WD-2TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:WD-2TB																																					
	639-15007	PCBA,MLB-C,64GB,HY-1TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:HY-1TB																																					
	639-15008	PCBA,MLB-C,64GB,HY-4TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:HY-4TB																																					
	639-15009	PCBA,MLB-C,64GB,HY-512,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:HY-512																																					
	C	639-15010	PCBA,MLB-C,64GB,HY-8TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:HY-8TB																																				
		639-15011	PCBA,MLB-C,64GB,TS-1TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:TS-1TB																																				
		639-15012	PCBA,MLB-C,64GB,TS-4TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:TS-4TB																																				
639-15013		PCBA,MLB-C,64GB,TS-512,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:TS-512																																					
639-15014		PCBA,MLB-C,64GB,TS-8TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:TS-8TB																																					
639-15015		PCBA,MLB-C,64GB,WD-1TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:WD-1TB																																					
639-15016		PCBA,MLB-C,64GB,WD-2TB,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_64G,SSD:WD-2TB																																					
939-10769		PCBA,MLB-C,SOCKET,SOC,X2723	BOM_BASE,BOM_DEV,ALTERNATE,SOC:SOCKET,SSD:NOSSE																																					
B	939-10770	PCBA,MLB-C,NO SOC,X2723	BOM_BASE,BOM_DEV,SSD:8L-DCDC,NAND:SOCKET																																					
	939-10908	PCBA,MLB-C,RF Test,X2723	RF-TEST,PCB																																					
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	<table><tr><td colspan="2">SYNC_MASTER=T668_MLB_5_7_0</td><td colspan="2">SYNC_DATE=07/20/2020</td></tr><tr><td colspan="4">PAGE TITLE</td></tr><tr><td colspan="4">BOM VARIANT TABLES</td></tr><tr><td colspan="2" rowspan="2"> Apple Inc.</td><td>DRAWING NUMBER</td><td>051-06558</td><td>SIZE</td></tr><tr><td>REVISION</td><td colspan="2">2.0.0</td></tr><tr><td colspan="2" rowspan="4">NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED</td><td>BRANCH</td><td colspan="2"></td></tr><tr><td>PAGE</td><td colspan="2">603 OF 998</td></tr><tr><td>SHEET</td><td colspan="2">153 OF 156</td></tr><tr><td colspan="2"></td></tr></table>								SYNC_MASTER=T668_MLB_5_7_0		SYNC_DATE=07/20/2020		PAGE TITLE				BOM VARIANT TABLES				 Apple Inc.		DRAWING NUMBER	051-06558	SIZE	REVISION	2.0.0		NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH			PAGE	603 OF 998		SHEET	153 OF 156		
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DES	COMMENTS:	138S0863	138S0853	ANY	ALL	<RDAR://56380033>	152S00398	152S00204	ANY	ALL	<RDAR://56380033>	152S00963	152S00885	ANY	ALL	<RDAR://56380033>	138S00047	138S00073	ANY	ALL	<RDAR://56380033>	152S01317	152S01268	ANY	ALL	<RDAR://57328156>	107S00087	107S00029	ANY	ALL	<RDAR://56380033>	107S00090	107S00055	ANY	ALL	<RDAR://56380033>	107S00373	107S00365	ANY	ALL	<RDAR://56380033>	128S00026	128S00011	ANY	ALL	<RDAR://56380033>	128S00087	128S00011	ANY	ALL	<RDAR://56380033>	128S00031	128S00011	ANY	ALL	<RDAR://56380033>	128S00039	128S00038	ANY	ALL	<RDAR://56380033>	128S0302	128S00038	ANY	ALL	<RDAR://56380033>	128S00065	128S00067	ANY	ALL	<RDAR://56380033>	128S00094	128S00067	ANY	ALL	<RDAR://56380033>	128S0364	128S0264	ANY	ALL	<RDAR://56380033>	152S00198	152S00680	ANY	ALL	<RDAR://56380033>	152S00383	152S00680	ANY	ALL	<RDAR://56380033>	152S00708	152S00265	ANY	ALL	<RDAR://56380033>	152S00390	152S00265	ANY	ALL	<RDAR://56380033>	152S00997	152S00476	ANY	ALL	<RDAR://56380033>	152S00367	152S01248	ANY	ALL	<RDAR://56380033>	376S00303	376S00012	ANY	ALL	<RDAR://56380033>	376S00204	376S00203	ANY	ALL	<RDAR://56380033>	376S00227	376S00203	ANY	ALL	<RDAR://56380033>	376S00226	376S00203	ANY	ALL	<RDAR://56380033>	376S00281	376S1147	ANY	ALL	<RDAR://56380033>	376S00007	376S1179	ANY	ALL	<RDAR://56380033>	376S00228	376S1179	ANY	ALL	<RDAR://56380033>	138S0789	138S0941	ANY	ALL	<RDAR://56380033>	107S00071	107S00053	ANY	ALL	<RDAR://56380033>	138S00332	138S00328	ANY	ALL	<RDAR://57328643>	152S00343	152S00839	ANY	ALL	<RDAR://57238826>	152S01090	152S01085	ANY	ALL	<RDAR://57230783>	ENOISE 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